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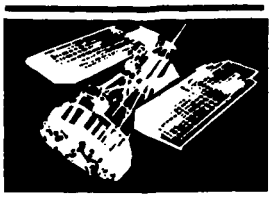
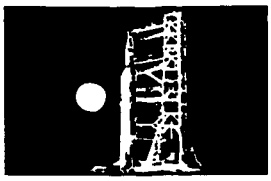
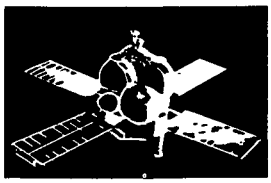
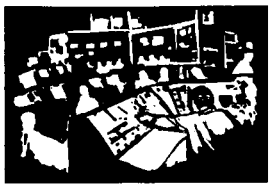
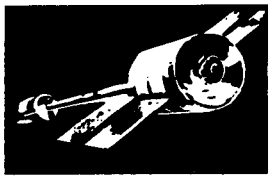
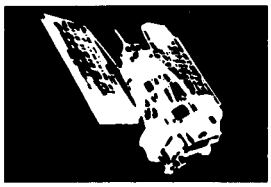
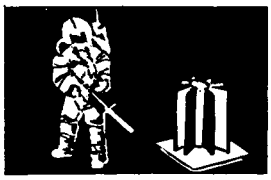
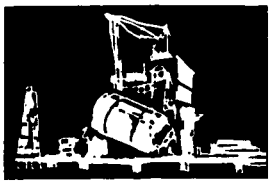

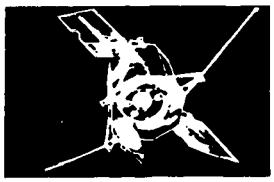

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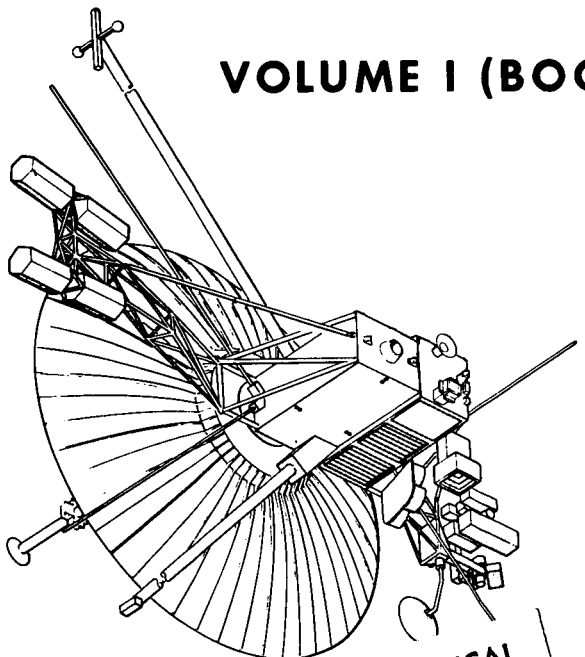
POWER CONDITIONING EQUIPMENT FOR A THERMOELECTRIC OUTER PLANET SPACECRAFT

JPL CONTRACT 952536

VOLUME I (BOOK 2)



GENERAL ELECTRIC COMPANY
SPACE DIVISION
PHILADELPHIA, PENNSYLVANIA

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"THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY, AS SPONSORED BY THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION UNDER CONTRACT NAS 7-100."

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ABSTRACT

This final report covers the significant activities associated with the design and development of Power Conditioning Equipment (PCE) for the Thermoelectric Outer Planet Spacecraft (TOPS) program. The work was performed under JPL Contract No. 952536 during the period from April 1969 through December 1971. During this period four quarterly technical reports were issued along with biweekly progress reports and numerous topical reports. This final report has assembled the more significant results of this overall effort.

One major aspect of the program included the design, assembly and test of various breadboard power conditioning elements. Among others these included a quad-redundant shunt regulator, a high voltage (~ 3500 vdc) Traveling Wave Tube dc-to-dc converter, two-phase gyro inverters and numerous solid-state switching circuits. Toward the end of the development effort many of these elements were arranged in a typical subsystem configuration and tests were conducted which demonstrated basic element compatibility.

In parallel with the development of the basic power conditioning elements, system studies were continued during the entire effort. As new mission related data became available from JPL, the design effort for the PCE was examined and a suitable system configuration was gradually evolved. The salient features of the selected power subsystem configuration are as follows:

- The PCE regulates the power from the radioisotope thermoelectric generator (RTG) power source at 30 vdc by means of a quad-redundant shunt regulator.
- 30 vdc power is used by certain loads, but is more generally inverted and distributed as square-wave ac power.
- A protected bus is used to assure that power is always available to the Control Computer Subsystem (CCS) to permit corrective action to be initiated in response to fault conditions.
- Various levels of redundancy are employed to provide high subsystem reliability.

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GLOSSARY

A/C	Attitude Control Subsystem
AEC	Atomic Energy Commission
ASI	Amperes per Square Inch
BOM	Beginning of Mission
CCS	Control Computer Subsystem
CDS	Command Decoder Subsystem
CG	Command Generator
CMMA	Ceramic Metalized Multigate Array
CT	Current Throttle
CTSS	Current Throttle Steering Switch
DPDT	Double Pole - Double Throw
DVM	Digital Volt Meter
EMC	Electromagnetic Compatibility
EOM	End of Mission
FD&C	Fault Detection and Correction
FMECA	Failure Mode, Effect, and Criticality Analysis
I/O	Input - Output
KHz	Kilo Hertz
LVCO	Low Voltage Cutoff
MB	Main Bus
Mev	Million Electron Volts
MHW	Multi-Hundred Watt
MVFD	Majority Vote Failure Detector
MPS	Measurement Processor Subsystem
OSE	Operations Support Equipment
PB	Protected Bus
PCE	Power Conditioning Equipment
PS	Power Supply
R_{ft}	Failure Tolerant Reliability
R_{pow}	100% Main Bus Power Reliability
RDA	Remote Decoder Array

RFS	Radio Frequency Subsystem
RTG	Radioisotope Thermoelectric Generator
S/C	Spacecraft
SEQ	Sequence
SRP	Shunt Resistor Panel
SW	Switch
TARP	Test and Repair Processor
T/C	Thermal Control Subsystem
TCM	Trajectory Correction Maneuver
TOPS	Thermoelectric Outer Planet Spacecraft
T/R	Transformer - Rectifier
TSS	Timing Synchronizer Subsystem
TTL	Transistor - Transistor Logic
TWT	Traveling Wave Tube

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SECTION 5
BREADBOARD CIRCUIT DESIGN

The detailed design and breadboard test results of those circuits investigated for the functions of the Power Conditioning Equipment are presented in the following sections. Also included is a detailed Failure Modes, Effect, and Criticality Analysis (FMECA) for those circuits selected for the baseline design.

5.1 CURRENT THROTTLE

5.1.1 FUNCTIONAL REQUIREMENTS

The Current Throttle (CT) is to provide a path to the Main Bus (MB) such that after the Protected Bus (PB) loads are satisfied, the remaining power of RTG No. 1 can be used by the MB loads (see Figure 5.1-1). This is to be accomplished by limiting the current to the MB in order to maintain the PB voltage. The CT is to meet the requirements of Table 5.1-1 while operating in two modes: a passing mode when the MB voltage is within specification; and a limiting mode when failures cause the MB voltage to drop below specification.

Table 5.1-1. Current Throttle Requirements *

CT Operating Mode	Input Voltage (vdc)	MB Voltage (vdc)	Pass Current (amperes)	Efficiency (Percent)
Pass	30.3 to 33.3	30.0 $\pm$ 0.30	0 to 5	95 @ 3 amperes
Limit	30.50 $\pm$ 0.30	0 to 29.7	0.9 to 3.5	--

* These functional requirements are those to which the breadboard was designed and tested. Since the breadboard testing, the theory of operation has remained the same with a change to the input voltage requirement.

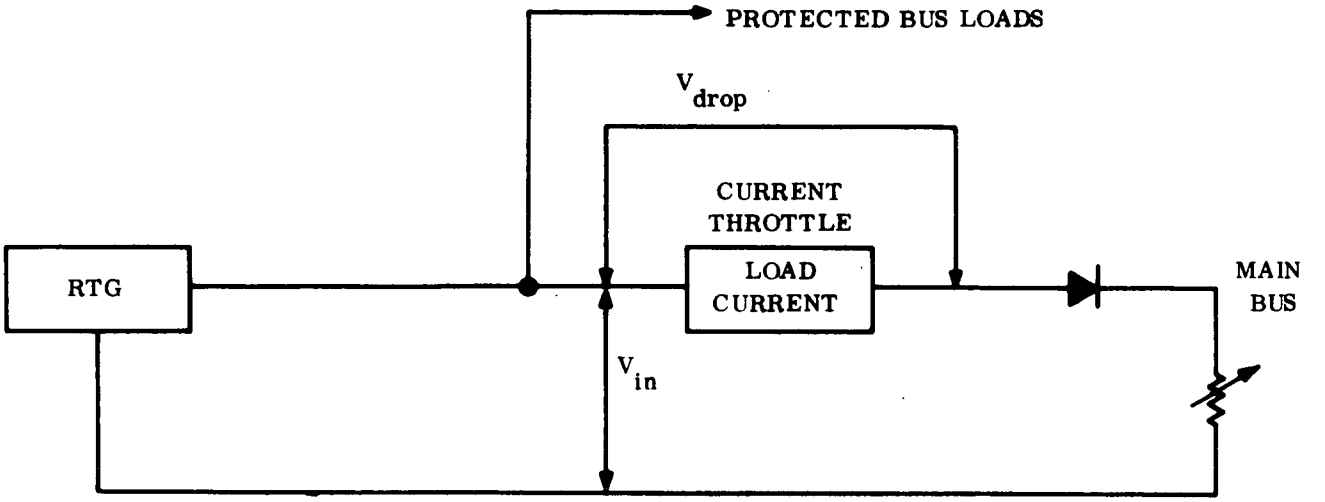


Figure 5.1-1. Current Throttle Interface Block Diagram

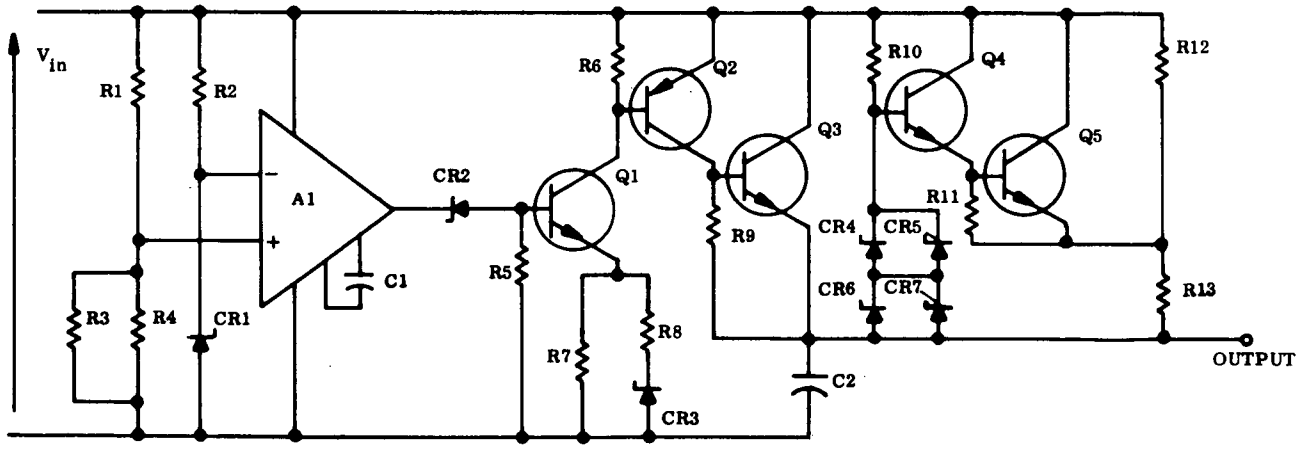


Figure 5.1-2. Current Throttle No. 2 Schematic

5.1.2 DESIGN DESCRIPTION

The Current Throttle shown schematically in Figure 5.1-2 is primarily a series regulator that senses its input rather than output voltage. It consists of a reference (CR1), a sense circuit (R1, R3, R4), a high gain amplifier (A1), current amplifiers (Q1, Q2), and the pass element (Q3).

When operating in the pass mode, the A1 output is high causing Q3 to be near saturation. A decrease in the output voltage would lower the input due to the small voltage drop across Q3. This then causes operation in the limit mode. A decrease in V_{in} reduces the output of A1 and results in a decrease of base drive to Q3. This results in an increase in voltage drop across Q3 which maintains the CT input voltage (V_{in}).

When in the limit mode, the gain of Q3 increases as it begins operating in its linear region. The network R7, R8, C3 reduces Q1 gain to prevent it and the amplifier A1 from operating to their cut-off regions where Q3 gain increases.

To reduce the dissipation in Q3 when in the limit mode, a current generator circuit was added which shunts slightly less than the minimum current the RTG can provide to the Main Bus. Two configurations of the current generator were tested. Configuration A and Configuration B were designed to bypass 3 amperes and 0.9 ampere respectively.

A quad arrangement of zener diodes was used in the current generator to prevent a single failure from drastically altering the bypassed current.

There is little thermal stress on the CT elements when operating in the pass mode. During the limit mode, however, it is possible that Q3 could dissipate as much as 80 watts. This possibly will elevate the junction temperature above the steady state maximum imposed for reliability, but duration of the limit mode operation is restricted by failure correction mechanisms to less than 1 second.

C

Temperatures obtainable in the transistor when packaged for flight cannot be determined until an actual mechanical design permits calculation of thermal resistances. It is felt if Q3 junction temperature does not exceed 200°C during the short high power mode, this Current Throttle design is adequate.

5.1.3 TEST RESULTS

The setup as shown in Figure 5.1-3 was used to test a development breadboard (CT No. 1) and a quality breadboard (CT No. 2) over the temperature range of -10 to +100°C. Dynamic response of CT No. 1 was determined using the setup of Figure 5.1-4.

The development breadboard was Vector-board constructed with the power transistors mounted to finned heat sinks, while the quality breadboard was mounted in a 7 x 9 x 2 inch aluminum chassis.

5.1.3.1 Development Breadboard (CT No. 1)

The schematic of CT No. 1 is shown in Figure 5.1-5.

The CT output was loaded to cause operation in the limit mode. Figure 5.1-6, which presents the effect on terminal voltage as the temperature is varied, shows that the terminal voltage variation is directly related to the zener diode (IN 827) change with temperature. The input voltage requirement of Table 5.1-1 was met. During this test, the voltage drop across the Current Throttle was varied at each temperature to determine the change in regulation. These results are summarized on the following chart.

Temp °C	-10	+10	+25	+40	+100
V_{drop} range	1.5 to 30.0	1.5 to 30.0	1.5 to 30.0	1.5 to 30.0	1.5 to 24.0
ΔV_{reg} over range	0.054	0.058	0.095	0.088	0.017

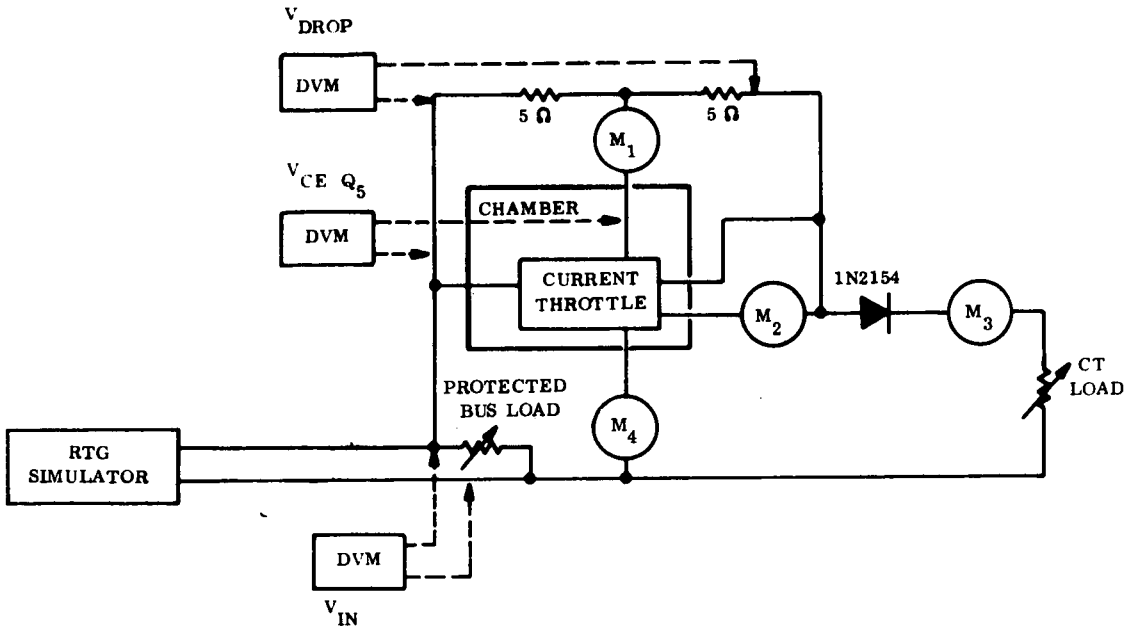


Figure 5.1-3. Temperature Test Setup

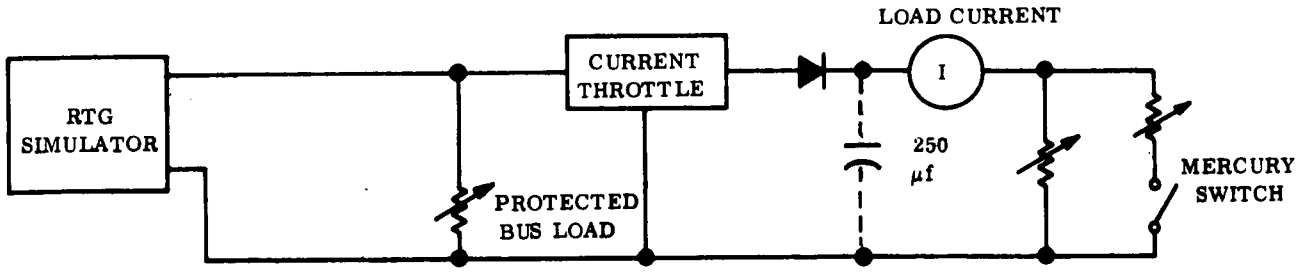


Figure 5.1-4. Dynamic Test Setup

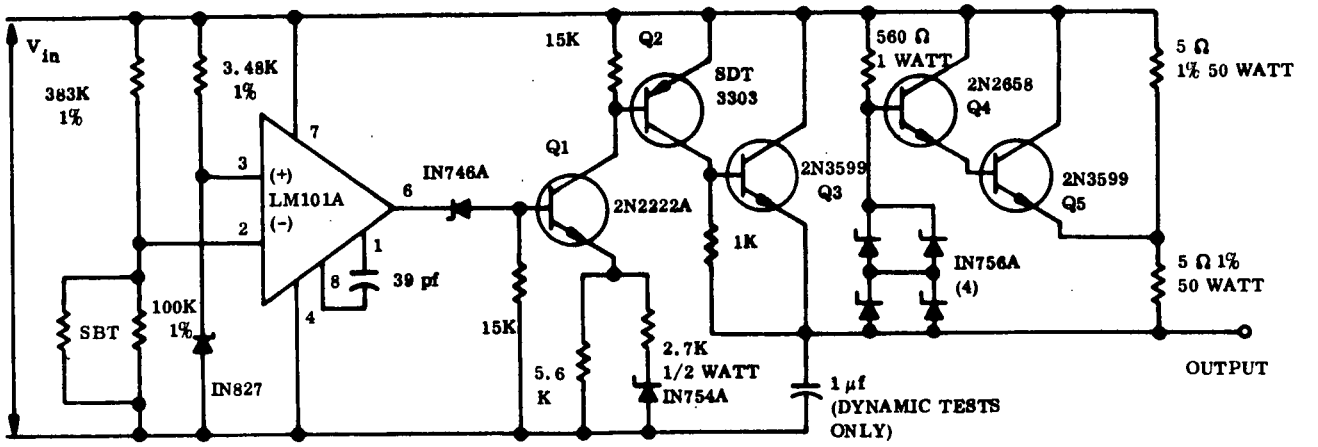


Figure 5.1-5. Current Throttle No. 1 Schematic (Development Breadboard)

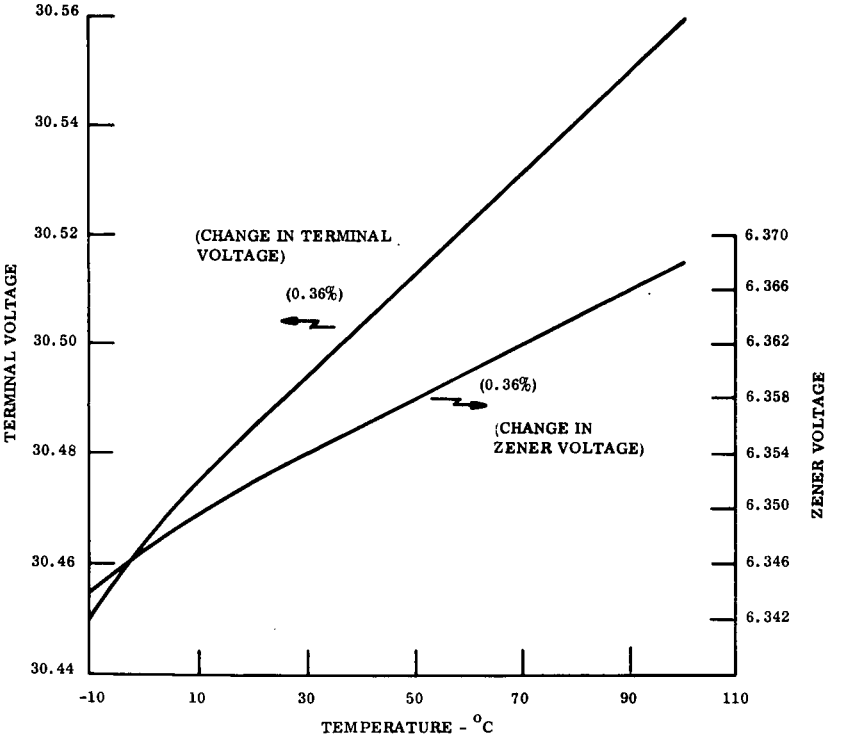


Figure 5.1-6. Current Throttle No. 1 Regulation Versus Temperature

The CT power dissipation while operating in the pass mode was calculated:

$$\text{Power Dissipation} = (V_{drop} \times I_{load}) + (V_{in} \times \text{loss current})$$

These results were plotted for various load current in Figure 5.1-7. This data was used to determine efficiency in the pass mode as follows:

$$\text{Percent Efficiency} = \frac{(I_L \times V_{in}) - \text{Power Dissipation}}{I_L \times V_{in}} \times 100$$

Efficiency as shown on Figure 5.1-8 exceeded the requirement of 95 percent at 3 amperes.

Next, the CT voltage drop in the pass mode was measured as load current (current through CT) was varied. The results are shown in Figure 5.1-9. Since values higher than anticipated were measured, a bench test shown as "Free Room Air" was performed. The data identified as "Free Room Air Including Wires" was measured at the same point as the temperature chamber voltage drop was measured. The effect of the wiring is evident when the measurement point is moved to be directly across the pass transistor Q3 as shown by the data titled "Free Room Air Across Pass Transistor." The difference between the two curves represent about 0.03 ohms of wiring. Consequently, the voltage drop, power dissipation and efficiency results include some line loss.

The power dissipation in the pass transistor Q3 and the constant current transistor Q5 is shown in Figure 5.1-10 when operating in the limit mode. In this case, the constant current generator was in Configuration A which shunts 3 amperes.

Dynamic tests of CT No. 1 were performed to measure the response to step loading the output which causes transition from the pass mode to the limit mode of operation. Also, effect of varying the compensation of the high gain amplifier A1 on the CT response was recorded on Figure 5.1-11. The minimum compensation required for stability was 10 picofarads.

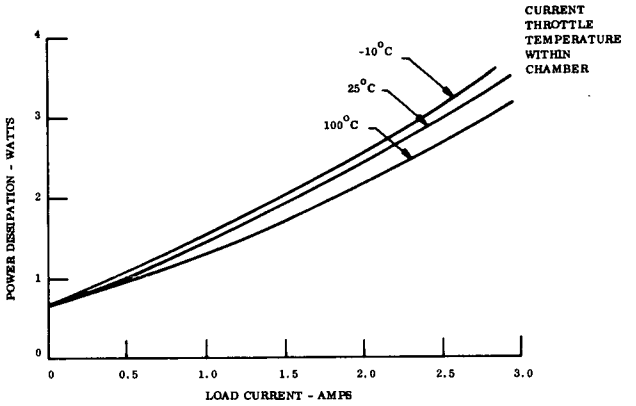


Figure 5.1-7. Current Throttle No. 1 Power Dissipation versus Load Current (Pass Mode)

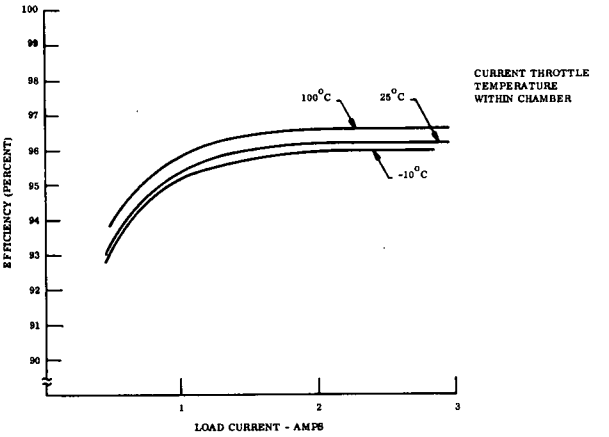


Figure 5.1-8. Current Throttle No. 1 Efficiency versus Load Current

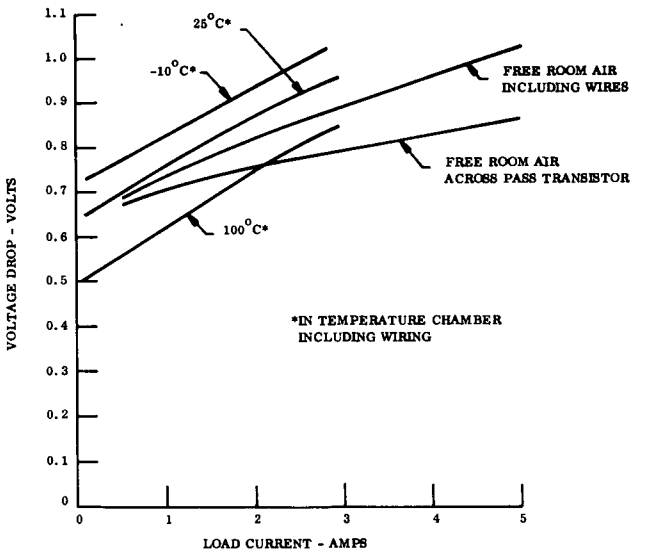


Figure 5.1-9. Current Throttle No. 1 Voltage Drop versus Load Current

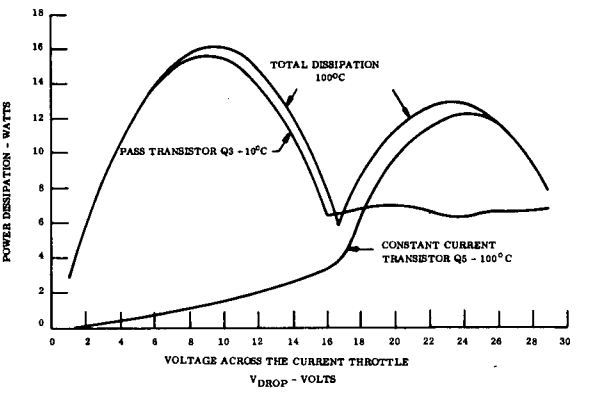
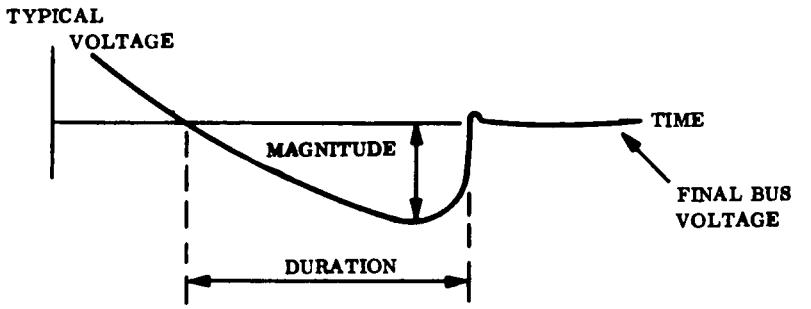


Figure 5.1-10. Current Throttle No. 1 Power Transistors Maximum Power Dissipation



Initial Current (amps)	V_{drop} Final (volts)	Compensation (pf)	Magnitude (volts)	Duration (μs)
2.90	5	10	0.13	122
2.90	5	20	0.20	165
2.90	5	39	0.27	235
2.90	15	10	0.45	46
2.90	15	20	0.63	74
2.90	15	39	0.98	118
< 0.01	5	10	0.15	115
< 0.01	5	20	0.20	175
< 0.01	5	39	0.28	250
< 0.01	15	10	0.47	50
< 0.01	15	20	0.60	76
< 0.01	15	39	1.02	125

Figure 5.1-11. Compensation Tradeoff and Undershoot Results (Data Interpreted from Photographs)

5.1.3.2 Quality Breadboard (CT No. 2)

The schematic of CT No. 2 was the same as CT No. 1 except a LM 208 was used in place of the LM 101A operational amplifier.

Two constant current sections were tested by changing the values of R12 and R13. Configuration A identifies the 3 ampere and Configuration B the 0.9 ampere unit.

The results of regulation tests over the temperature range show that both were within the specified requirement (see Figure 5.1-12).

Figures 5.1-13 and 5.1-14 show the voltage drop across the CT when operating in the pass mode. As with the same test performed on CT No. 1, it was found that these measurements included about 0.04 ohms of wiring drop and therefore are slightly larger than actual. This is demonstrated by the curve entitled Q3 Bench on Figure 5.1-14.

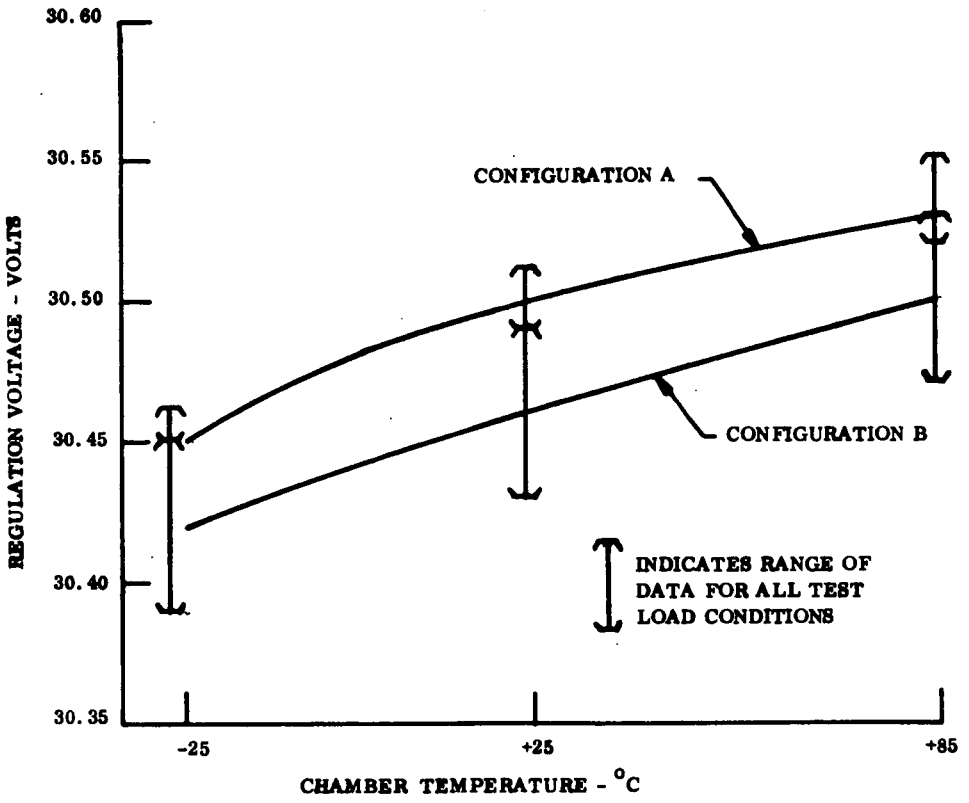


Figure 5.1-12. Current Throttle No. 2 Regulation versus Temperature

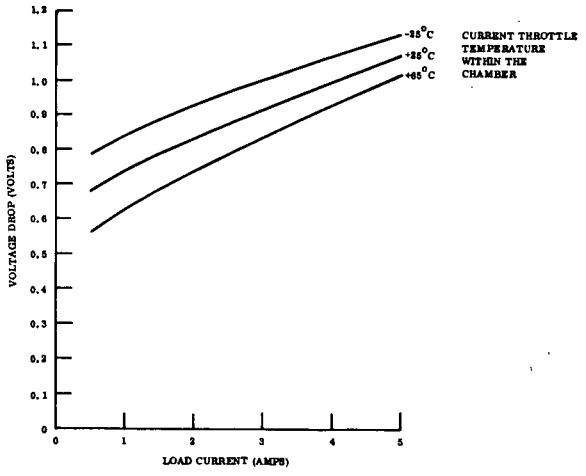


Figure 5.1-13. Current Throttle No. 2 Voltage Drop versus Load Current Configuration A

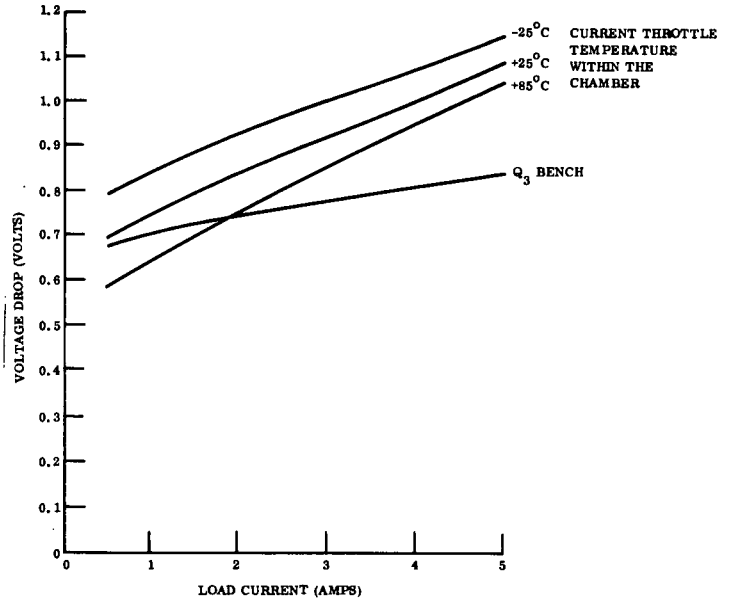


Figure 5.1-14. Current Throttle No. 2 Voltage Drop versus Load Current Configuration B

The power dissipation and efficiency were determined in the same manner as CT No. 1 and are shown on Figures 5.1-15 and 5.1-16.

5.1.4 FAILURE MODE, EFFECT, AND CRITICALITY ANALYSIS

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.1-2. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

5.1.4.1 Special Recommendations

When the Standby Current Throttle is switched on into an overvoltage condition on the Protected Bus due to an open failure of the main Current Throttle, it will turn on to load the bus and bring it into regulation within 500 microseconds. The LM208 op amp is rated for a maximum source voltage of 40 vdc which is below the 41 vdc transient overvoltage level expected on the Protected Bus. It is recommended that the LM208 be replaced by an LM101A which is rated for a higher source voltage.

5.1.4.2 Piece Part and Circuit Failure Rates

The following tabulation (Table 5.1-3) was derived using the Current Throttle schematic (Figure 5.1-2) and the approved piece part failure rates.

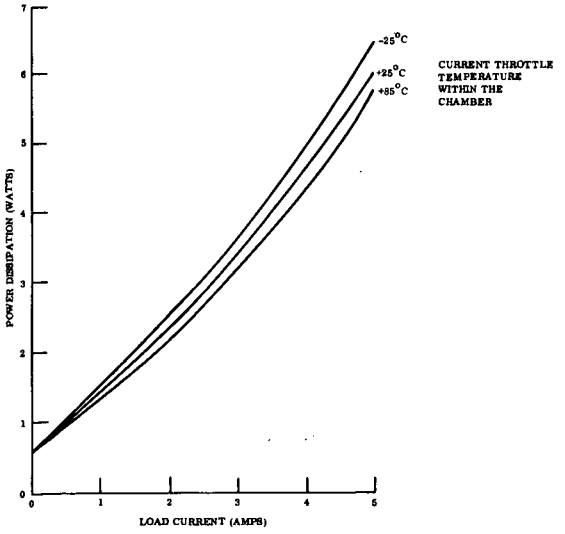


Figure 5.1-15. Current Throttle No. 2 Total Power Dissipation versus Load Current Configuration A

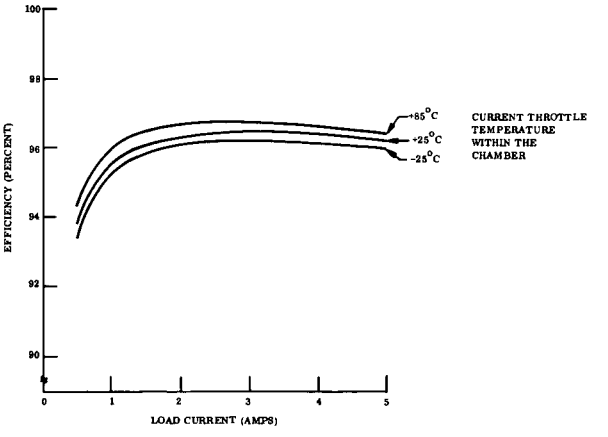


Figure 5.1-16. Current Throttle No. 2 Efficiency versus Load Current Configuration A

Table 5.1-2. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component CURRENT THROTTLE
Drawing No.

Prepared by R. ANDREWS

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	R1	RESISTOR	PART OF INPUT VOLTAGE SENSE DIVIDER	OPEN		REMOVES BASE DRIVE FROM PASS TRANSISTOR Q3 AND CAUSES CURRENT THROTTLING	PROTECTED BUS VOLTAGE RISES DUE TO UNLOADING RTG #1	C.T. STEERING SWITCH SENSES AND SWITCHES IN THE STANDBY CURRENT THROTTLE	
2	R2	RESISTOR	LIMITS CURRENT TO VOLTAGE REFERENCE CR1	OPEN		Op AMP OUTPUT WILL ALWAYS REMAIN HIGH. Q3 REMAINS ON EVEN WITH LOW INPUT VOLTAGE	NO EFFECT UNTIL MAIN BUS FAILURE PULLS DOWN THE PROTECTED BUS VOLTAGE.	C.T. STEERING SWITCH SENSES AND SWITCHES IN THE STANDBY CURRENT THROTTLE	SHORTED C.T.
3	R3	RESISTOR	PART OF INPUT VOLTAGE SENSE DIVIDER	OPEN		CHANGES THE OPERATING VOLTAGE RANGE. INPUT VOLTAGE MUST DROP LOWER NOW FOR CURRENT THROTTLING.	NO EFFECT UNTIL MAIN BUS FAILURE PULLS DOWN THE PROTECTED BUS VOLTAGE	C.T. STEERING SWITCH SENSES AND SWITCHES IN THE STANDBY CURRENT THROTTLE	SHORTED C.T.
4	R4	RESISTOR	PART OF INPUT VOLTAGE SENSE DIVIDER	OPEN		CHANGES THE OPERATING VOLTAGE RANGE. INPUT VOLTAGE MUST DROP LOWER NOW FOR CURRENT THROTTLING.	NO EFFECT UNTIL MAIN BUS FAILURE PULLS DOWN THE PROTECTED BUS VOLTAGE	C.T. STEERING SWITCH SENSES AND SWITCHES IN THE STANDBY CURRENT THROTTLE	SHORTED C.T.
5	R5	RESISTOR	Q1 LEAKAGE RESISTOR	OPEN		IF Q1 HAS HIGH LEAKAGE, GAIN TO Q3 COULD BE SUFFICIENT TO KEEP CT FULL ON AND NOT THROTTLE.	CURRENT THROTTLE WILL NOT WORK WHEN MAIN BUS VOLTAGE DROPS	C.T. STEERING SWITCH SENSES AND SWITCHES IN THE STANDBY CURRENT THROTTLE	SHORTED C.T.
6	R6	RESISTOR	Q2 LEAKAGE RESISTOR	OPEN		IF Q2 HAS HIGH LEAKAGE, GAIN TO Q3 COULD BE SUFFICIENT TO KEEP CT FULL ON AND NOT THROTTLE.	CURRENT THROTTLE WILL NOT WORK WHEN MAIN BUS VOLTAGE DROPS	C.T. STEERING SWITCH SENSES AND SWITCHES IN THE STANDBY CURRENT THROTTLE	SHORT C.T.

Table 5.1-2. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component CURRENT THROTTLE
Drawing No. _____

Prepared by _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
7	R7	RESISTOR	DETERMINES Q2-Q3 DRIVE WHEN CT IS LIMITING	OPEN		REDUCTION IN FREQUENCY RESPONSE DUE TO REDUCTION IN FEEDBACK CURRENT	SLOWER RESPONSE TO CHANGE IN PROTECTED BUS VOLTAGE. LARGER TRANSIENT DURATION.	NONE	
8	R8	RESISTOR	DETERMINES GAIN OF Q1 WHEN NOT LIMITING	OPEN		IF NOT SUFFICIENT GAIN IN Q2 - Q3, PB VOLTAGE WILL RISE.	NO EFFECT UNTIL PB VOLTAGE EXCEEDS SPEC. VALUE	C.T. STEERING SWITCH SELECTS STANDBY C.T.	
9	R9	RESISTOR	Q3 LEAKAGE RESISTOR	OPEN		COULD PREVENT THROTTLING IF Q3 LEAKAGE CURRENT IS HIGH	NO EFFECT UNTIL MAIN BUS FAILURE PULLS DOWN THE PROTECTED BUS VOLTAGE	C.T. STEERING SWITCH SELECTS STANDBY C.T.	SHORT C.T.
10	R10	RESISTOR	CURRENT LIMITER FOR Q4	OPEN		CONSTANT CURRENT SECTION OF Q4 - Q5 FAILS TO PERFORM	CAUSES EXCESS DISSIPATION IN Q3 PASS ELEMENT WHEN THROTTLING. Q3 MIGHT FAIL	C.T. STEERING SWITCH SELECTS STANDBY C.T.	
11	R11	RESISTOR	Q5 LEAKAGE RESISTOR	OPEN		IF Q5 LEAKAGE IS HIGH, TOO MUCH CURRENT COULD BE PASSED TO THE MAIN BUS UNDER THROTTLING CONDITIONS	P.B. VOLTAGE MIGHT DROP BELOW SPEC.	C.T. STEERING SWITCH SELECTS STANDBY C.T.	
12	R12	RESISTOR	POWER BYPASS	OPEN		INCREASES POWER DISSIPATION IN Q4 - Q5 WHEN THROTTLING	NO EFFECT UNLESS Q4 - Q5 FAILS		See Item 22
13	R13	RESISTOR	POWER BYPASS	OPEN		ALL CURRENT WILL PASS THRU Q3 WHEN THROTTLING	CAUSES INCREASE IN DISSIPATION OF Q3.(150 WATTS) PROBABLY WOULD FAIL.	C.T. STEERING SWITCH SELECTS STANDBY C.T.	
14	CR1	ZENER DIODE	VOLTAGE REFERENCE	OPEN		Op AMP OUTPUT GOES LOW, REMOVING BASE DRIVE FROM Q3 AND CAUSES CURRENT THROTTLING	PROTECTED BUS VOLTAGE RISES DUE TO UNLOADING RTG #1	C.T. STEERING SWITCH SELECTS STANDBY C.T.	OPEN C.T.
				SHORT		Op AMP OUTPUT WILL NEVER GO LOW.	C.T. WILL NOT THROTTLE IF MB GOES DOWN		SHORTED C.T.

Table 5.1-2. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component CURRENT THROTTLE
Drawing No.

Prepared by

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
15	CR2	ZENER DIODE	MINIMUM Op AMP OUTPUT VOLTAGE WOULD NOT ALLOW Q1 TO CUT-OFF. THIS ZENER VOLTAGE DROP COMPENSATES FOR THAT	OPEN		LOSS OF BASE DRIVE TO Q1	C.T. FAILS OPEN CIRCUIT. WON'T PASS CURRENT TO MAIN BUS	C.T. STEERING SWITCH SELECTS STANDBY C.T.	OPEN C.T.
				SHORT		Q1 CANNOT BE COMPLETELY CUT-OFF WHEN THROTTLING	PROTECTED BUS VOLTAGE COULD DROP BELOW SPEC. IF MB FAULT IS LARGE		
16	CR3	ZENER DIODE	VOLTAGE REFERENCE FOR Q1 GAIN WHEN NOT LIMITING	OPEN		REDUCES BASE DRIVE TO Q2. IF NOT SUFFICIENT GAIN IN Q2 - Q3 PB VOLTAGE WILL RISE	NO EFFECT UNTIL PB VOLTAGE EXCEEDS SPEC. VALUE	C.T. STEERING SWITCH SELECTS STANDBY C.T.	
				SHORT		INCREASES GAIN OF Q1, Q1 COULD GO INTO CUT-OFF WHEN THROTTLING	RESPONSE TIME WOULD BE REDUCED WHEN COMING OUT OF THROTTLING MODE	NONE REQUIRED	
17	CR4 THRU CR7	ZENER DIODE	VOLTAGE REFERENCE FOR CONSTANT CURRENT SECTION	OPEN		CONSTANT CURRENT SECTION WOULD PASS TOO MUCH CURRENT WHEN THE MB VOLTAGE DROPS BELOW 15 VDC	PB VOLTAGE WOULD DROP SPEC.	C.T. STEERING SWITCH SELECTS STANDBY C.T.	THESE ZENER DIODES ARE IN A QUAD ARRANGMENT. FOR A FAILURE OPEN, TWO PARALLEL DIODES MUST FAIL OPEN FOR A FAILURE SHORT, TWO SERIES DIODES MUST FAIL SHORT
				SHORT		CURRENT PASSED BY THIS SECTION WOULD BE REDUCED WHEN THROTTLING, Q3 WOULD HAVE TO MAKE UP THE DIFFERENCE.	INCREASED POWER IN Q3 COULD CAUSE FAILURE.		

Table 5.1-2. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component CURRENT THROTTLE
Drawing No. _____

Prepared by _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
18	LM208	OPERATIONAL AMPLIFIER	COMPARES SAMPLED PB INPUT VOLTAGE WITH A REFERENCE VOLTAGE	OUTPUT HIGH		Q3 REMAINS FULL ON. NO THROTTLING IF THE MB VOLTAGE DROPS	PB VOLTAGE DROPS WHEN MB VOLTAGE FALLS	C.T. STEERING SWITCH SELECTS STANDBY C.T.	SHORT C.T.
				OUTPUT LOW		Q3 CUTS OFF. WON'T PASS CURRENT INTO MB	PB VOLTAGE GOES HIGH DUE TO INADEQUATE LOADING OF RTG		OPEN C.T.
19	Q1	TRANSISTOR	AMPLIFICATION OF O_p AMP SIGNAL	OPEN		Q3 CUTS OFF. WON'T PASS CURRENT INTO MB	PB VOLTAGE GOES HIGH DUE TO INADEQUATE LOADING OF RTG	C.T. STEERING SWITCH SELECTS STANDBY C.T.	OPEN C.T.
				SHORT		Q3 REMAINS FULL ON. NO THROTTLING IF THE MB VOLTAGE DROPS	PB VOLTAGE DROPS WHEN MB VOLTAGE FALLS.		SHORT C.T.
20	Q2	TRANSISTOR	AMPLIFICATION OF Q1 SIGNAL	OPEN		Q3 CUTS OFF. WON'T PASS CURRENT INTO MB	PB VOLTAGE GOES HIGH DUE TO INADEQUATE LOADING OF RTG	C.T. STEERING SWITCH SELECTS STANDBY C.T.	OPEN C.T.
				SHORT		Q3 REMAINS FULL ON. NO THROTTLING IF THE MB VOLTAGE DROPS.	PB VOLTAGE DROPS WHEN MB VOLTAGE FALLS		SHORT C.T.
21	Q3	TRANSISTOR	PASS SUFFICIENT CURRENT INTO THE MAIN BUS TO CONTROL THE PROTECTED BUS VOLTAGE	OPEN		MINIMAL CURRENT FLOW INTO MB VIA R12 R13.	PB VOLTAGE GOES HIGH DUE TO INADEQUATE LOADING OF RTG	C.T. STEERING SWITCH SELECTS STANDBY C.T.	OPEN C.T.
				SHORT		NO THROTTLING IF THE MB VOLTAGE DROPS	PB VOLTAGE DROPS WHEN MB VOLTAGE FALLS.		SHORT C.T.

Table 5. 1-2. Failure Mode, Effect and Criticality Analysis (Cont'd)

Subsystem POWER
Component CURRENT THROTTLE
Drawing No.

Prepared by

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
22	Q4 & Q5	TRANSISTOR	DARLINGTON ARRANGEMENT WHICH SHUNTS CURRENT PAST R12 WHEN OUTPUT IS LOW. REDUCES POWER DISSIPATION IN Q3 WHEN THROTTLING	OPEN		CONSTANT CURRENT SECTION WILL NOT PASS ENOUGH CURRENT INTO MB WHEN THROTTLING. Q3 MUST MAKE UP THE DIFFERENCE	CAUSES INCREASE IN DISSIPATION OF Q3 WHEN THROTTLING. Q3 MIGHT FAIL.	C.T. STEERING SWITCH SELECTS STANDBY C.T.	
				SHORT		CONSTANT CURRENT SECTION WILL PASS TOO MUCH CURRENT INTO MB WHEN MB VOLTAGE IS 16 VDC OR LESS.	PB VOLTAGE DROPS WHEN MB VOLTAGE IS LESS THAN 16 VDC		

Table 5.1-3. Failure Rate Calculations

Piece Part	Resistor -Carbon-		Resistor -Film-		Resistor -Power-		Diode -Zener-		Transistor -Signal-		Transistor -Power-		Operational Amplifier	
Failure Rate (x 10^6)	λ=0.001		λ=0.008		λ=0.090		λ=0.020		λ=0.020		λ=0.080		λ=0.200	
Failure Mode	Open	Short	Open	Short	Open	Short	Open	Short	Open	Short	Open	Short	Open	Short
Failure Mode Symbol	λo	λs	λo	λs	λo	λs	λo	λs	λo	λs	λo	λs	λo	λs
Failure Mode Probability	1.0	1.0	1.0	1.0	1.0	1.0	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Qauntity per Circuit	4	3	0	3	3	0	5	1	3	1	3	3	1	1
Cumulative Failure Rate	0.004	0.003	0	0.024	0.270	0	0.050	0.010	0.030	0.010	0.120	0.120	0.100	0.100

Failure Mode Totals	
$\lambda o_T = \Sigma \lambda o$	0.004 + 0.000 + 0.270 + 0.050 + 0.030 + 0.120 + 0.100 = 0.574
$\lambda s_T = \Sigma \lambda s$	0.003 + 0.024 + 0.000 + 0.010 + 0.010 + 0.120 + 0.100 = 0.267
λ_T	0.841 x 10^{-6} failures per hour

5.2 CURRENT THROTTLE STEERING SWITCH

5.2.1 FUNCTIONAL REQUIREMENTS (Figure 5.2-1)

The current throttle steering switch provides the power path through one of two current throttles. Normally, one is specified as prime, and the second throttle is selected only if the first one is known to have failed. The electronics of the steering switch senses the voltage on the Protected Bus to detect a current throttle failure. The second throttle is selected if the Protected Bus voltage exceeds 32.8 +0.3 volts or falls below 31.6 - 0.3 volts dc. The selection of either current throttle can be done by CCS command and the steering switch design must be such that no failure in the voltage detection circuitry overrides a subsequent command. To avoid erroneous switchover due to system transients, a 1 to 5 millisecond delay was required.

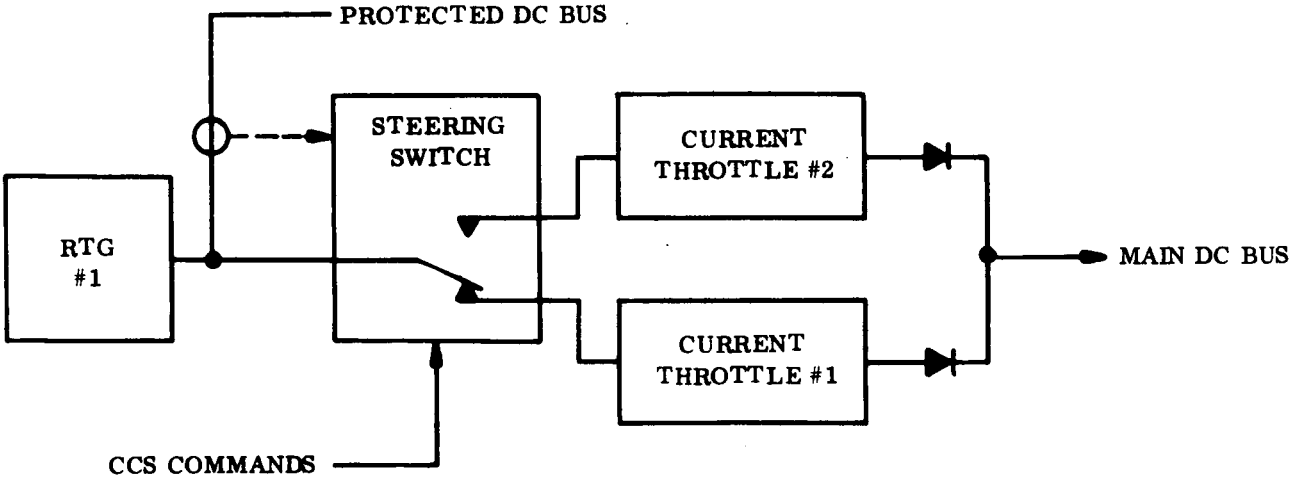


Figure 5.2-1. Current Throttle Steering Switch Interface Block Diagram

These functional requirements are those to which the breadboard was designed and tested. Since the breadboard testing, the theory of operation has remained the same with a change to the Protected Bus voltage levels at which the second current throttle is selected.

5.2.2 DESIGN DESCRIPTION (Figure 5.2-2)

The steering switch is simply a DPDT mag latch relay with coil drivers for command interface. An under/over voltage detector can also provide the select current throttle (CT) No. 2 command, capacitively coupled to provide greater than 10 milliseconds command pulse width, and permit command override reset to No. 1 despite a detector output.

Energy storage is provided for selecting CT No. 2 since a fault on the Main Bus will pull down the Protected Bus if the CT No. 1 has failed short. The 62 ohm resistor in the B+ line along with the 100 μf energy storage capacitor prevents damage to the amplifier due to the high voltage transient (50-60 volts) which occurs either when the RTG feeding the main bus is unloaded due to a CT failure open or during transfer of the steering relay.

5.2.3 TEST RESULTS

Two units (a breadboard and a qual unit) were performance tested from -20 to 85^{o}C ambient temperature. The relay coil (2 amp crystal can relay) was simulated with a 600 Ω resistor. The qual unit was constructed on a card and mounted with the current throttle qual unit.

The test setup is shown in Figure 5.2-3. The power supply voltage was slowly raised or lowered until the operational amplifier output went high and the corresponding bus voltage was recorded. The power supply was then slowly changed back toward the deadband until the operational amplifier returned to a low voltage and the corresponding bus voltage was recorded as the reset level.

Photographs of the output (simulated relay coil) voltage waveform were taken to analyze delay and pulse width. The operational amplifier was found to go high in less than 50 μs after a trip condition occurred on the bus, so the operational amplifier output was used to trigger the scope sweep for both delay and pulse width measurements.

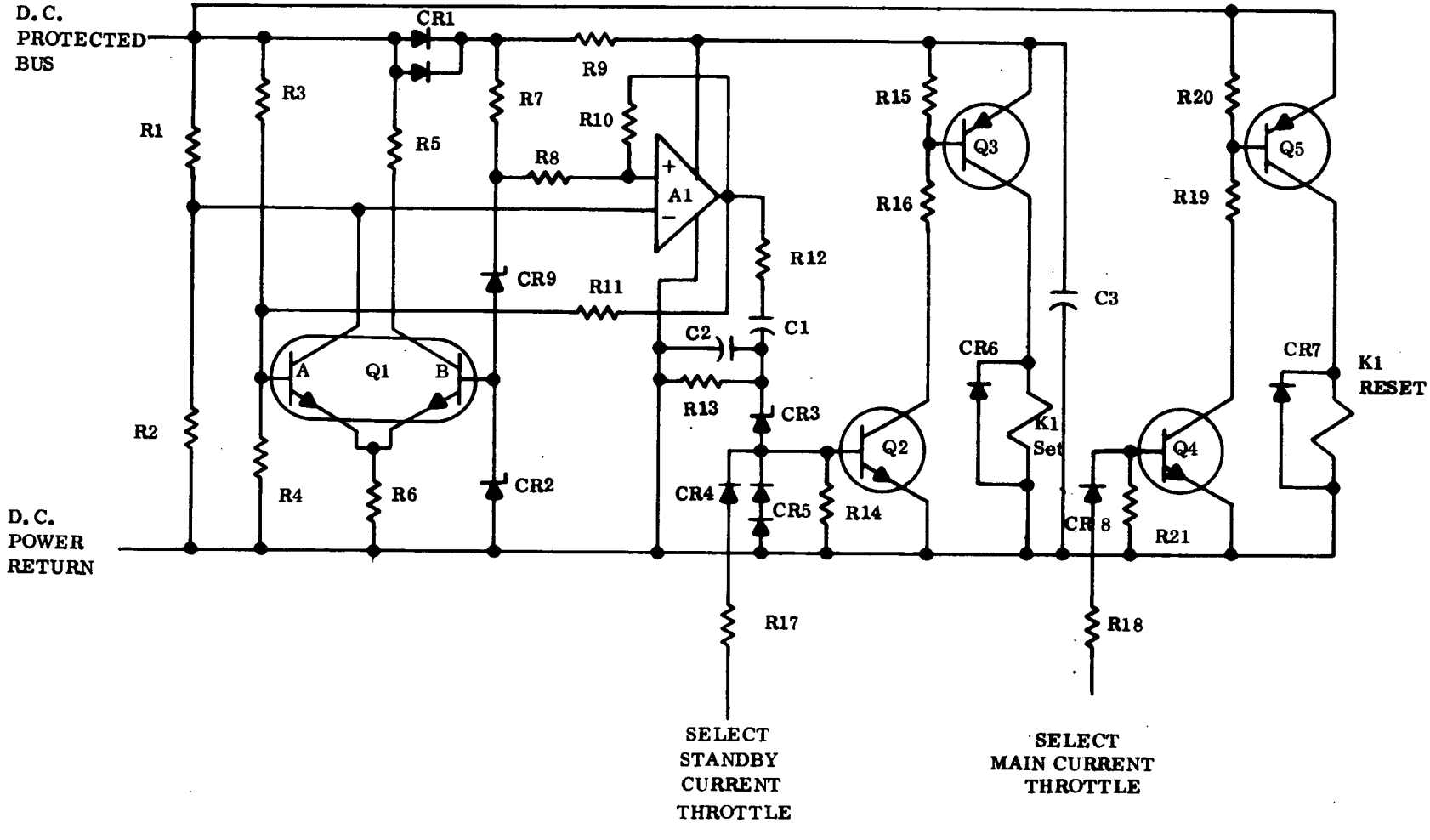


Figure 5.2-2. Current Throttle Steering Switch Flight Schematic

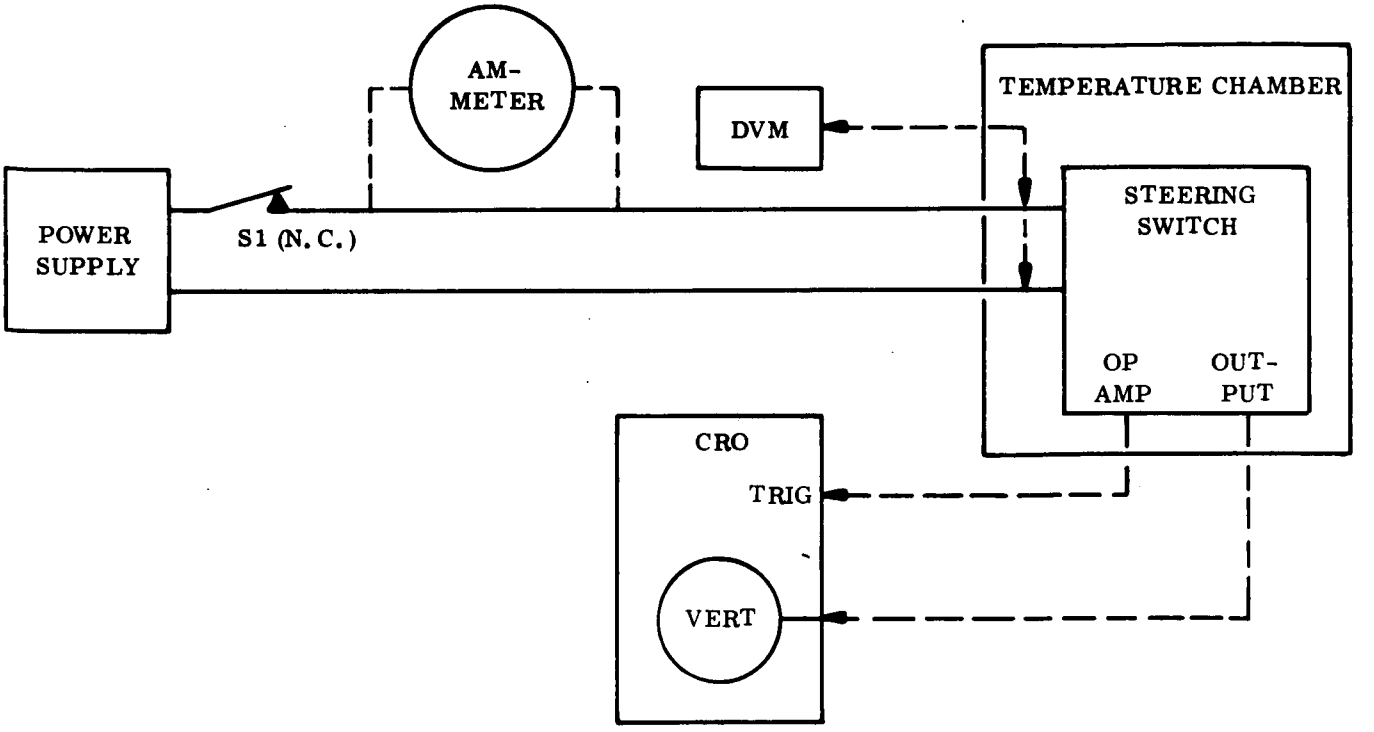


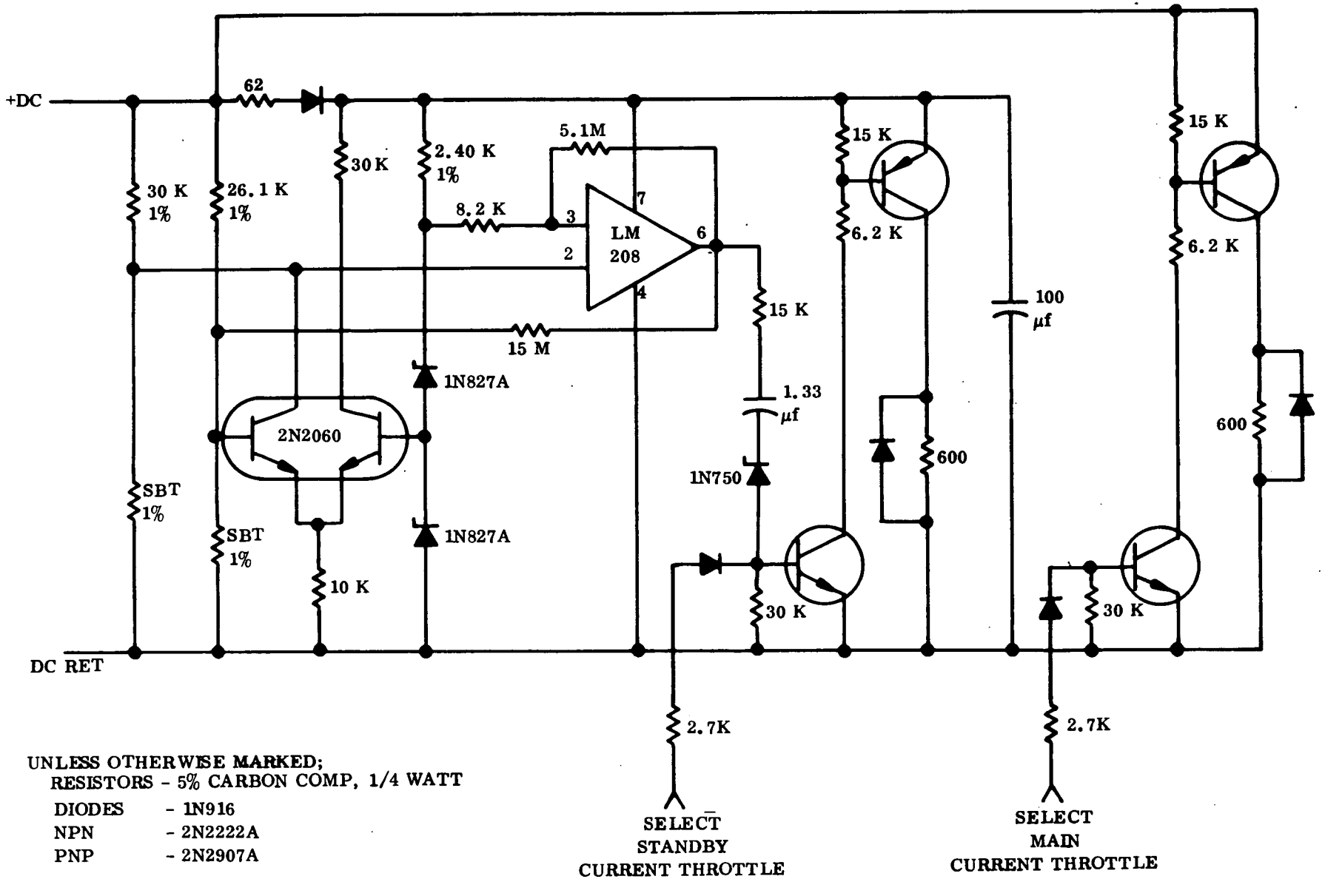
Figure 5.2-3. Current Throttle Steering Switch Test Setup

Photographs were taken of the delay for both high and low trip. Photographs were also taken of the output duration for low trip, and for low trip caused by opening the power line (S1) which tested the adequacy of the energy storage.

The power consumption was determined by measuring the dc current with a milliammeter at 32.0 volts. The meter was removed for trip tests.

Figures 5.2-4 and 5.2-5 are the schematics of the two units tested. The breadboard unit was tested before the delay requirement was imposed and the pulse width was far in excess of the desired 10 ms (34 ms at 25^{o}C). The trip points were also different from the qual unit due to a requirements revision, but the test still serves to demonstrate the design adequacy. The trip point results are given in Figure 5.2-6.

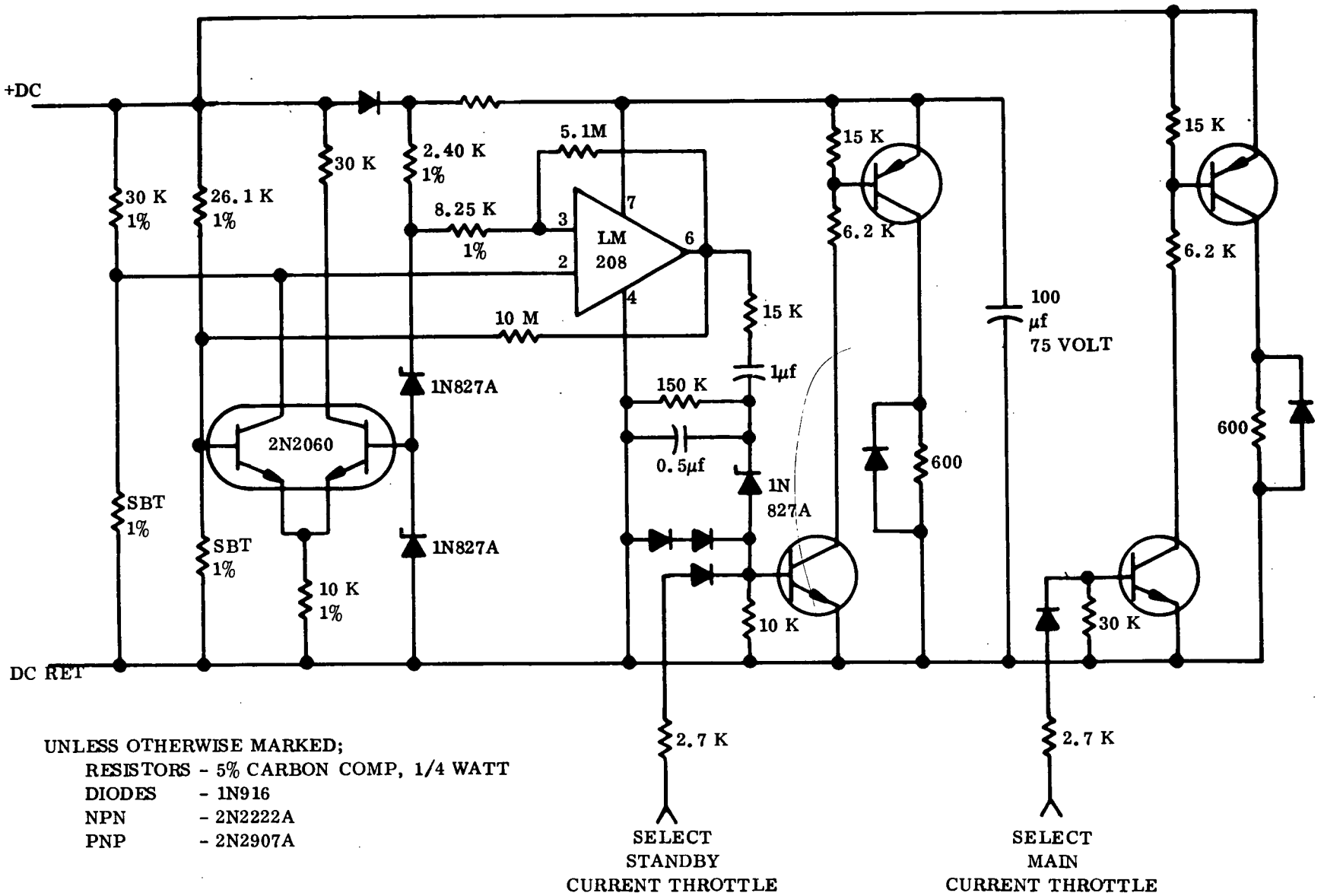
Several changes were made in the qual unit design (Figure 5.2-5) based on results of the breadboard unit tests and revised requirements. The delay circuit was added. The 62 Ω



UNLESS OTHERWISE MARKED;
RESISTORS - 5% CARBON COMP, 1/4 WATT

DIODES	- 1N916
NPN	- 2N2222A
PNP	- 2N2907A

Figure 5.2-4. Current Throttle Steering Switch Breadboard Schematic



UNLESS OTHERWISE MARKED;
RESISTORS - 5% CARBON COMP, 1/4 WATT
DIODES - 1N916
NPN - 2N2222A
PNP - 2N2907A

Figure 5.2-5. Current Throttle Steering Switch Qual Unit Schematic

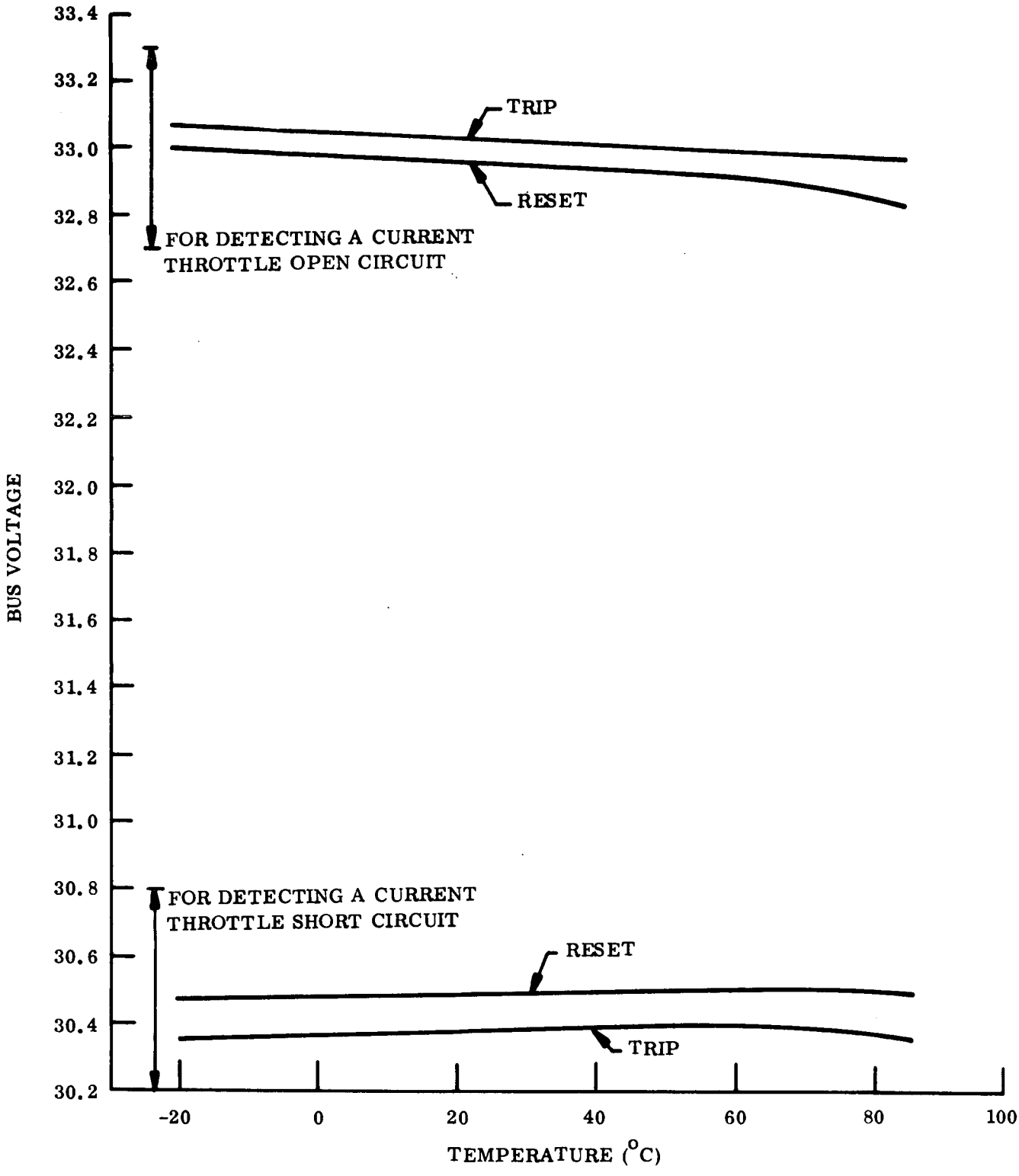


Figure 5.2-6. Current Throttle Steering Switch Trip Voltages - Breadboard

resistor was placed downstream in the power path from the zener current source to prevent the negative feedback through the reference which occurs when current drawn due to a response to a trip condition increased the voltage drop across the 62 Ω. The corresponding slight decrease in zener voltage which occurs in the breadboard configuration can cause oscillation at the trip point. The diff-amp collector was moved to the anode side of the blocking diode to preclude the waste of that current out of the energy storage capacitor in the event of severe undervoltage.

Figure 5.2-7 presents the summary of the qual unit test results. Delay times and pulse durations are taken from photographs of oscilliscope traces. Figure 5.2-8 graphically presents the trip point results versus specification. Carbon film resistors were used in the voltage sense dividers which probably accounts for the slope of the low trip point. The slope and amount of variation of the low trip point given in Figure 5.2-6, breadboard unit results, is consistent with tests done with the voltage sense divider located outside the temperature chamber.

	Temperature - °C				
Performance Function	-20	0	25	55	85
High Trip	32.82	32.82	32.81	32.81	32.79
High Trip Reset	32.76	32.75	32.75	32.74	32.73
Low Trip	31.49	31.54	31.60	31.74	31.80
Low Trip Reset	31.56	31.60	31.66	31.68	31.74
DC Supply Current @ 32.0 Volts	9.9 ma	10.0 ma	10.0 ma	10.1 ma	10.2 ma
DC Power ($32.0 \times I_{Supply}$)	317 mw	320 mw	320 mw	323 mw	326 mw
High Trip Time Delay	2.25 ms		2.25 ms		2.2 ms
Low Trip Time Delay	2.45 ms		2.4 ms		2.35 ms
Low Trip Output Pulse Width	24 ms		34 ms		41 ms
Power Turn Off Output Pulse Width	11.5 ms		13 ms		15.5 ms

Figure 5.2-7. Current Throttle Steering Switch Qual Unit Test Data Summary

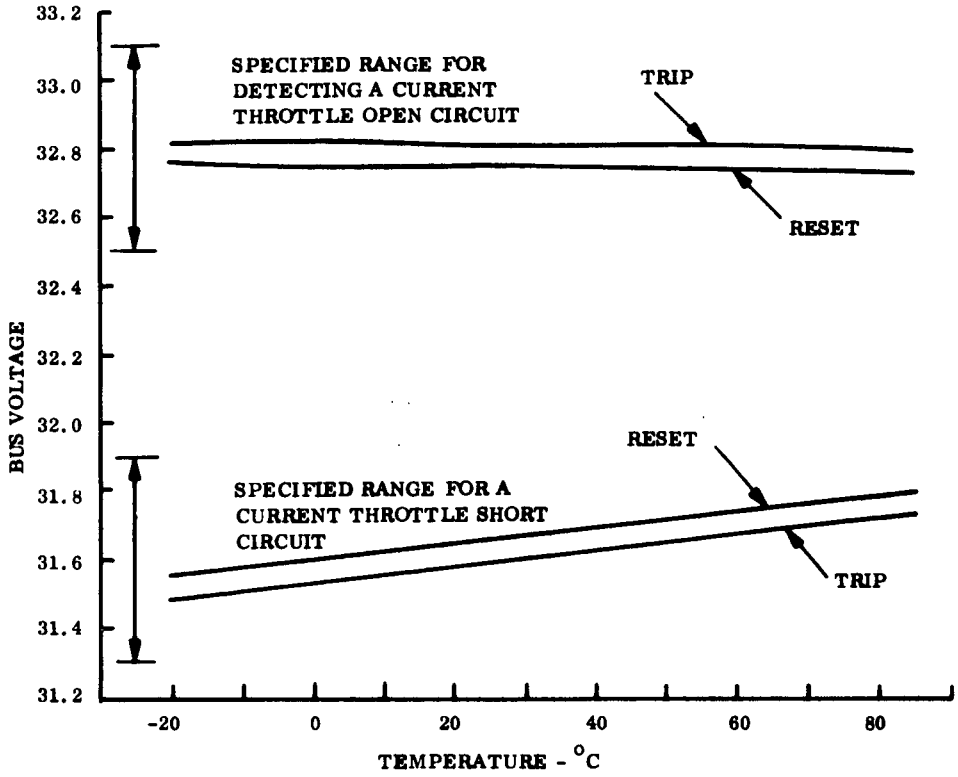


Figure 5.2-8. Current Throttle Steering Switch Performance - Qual Unit

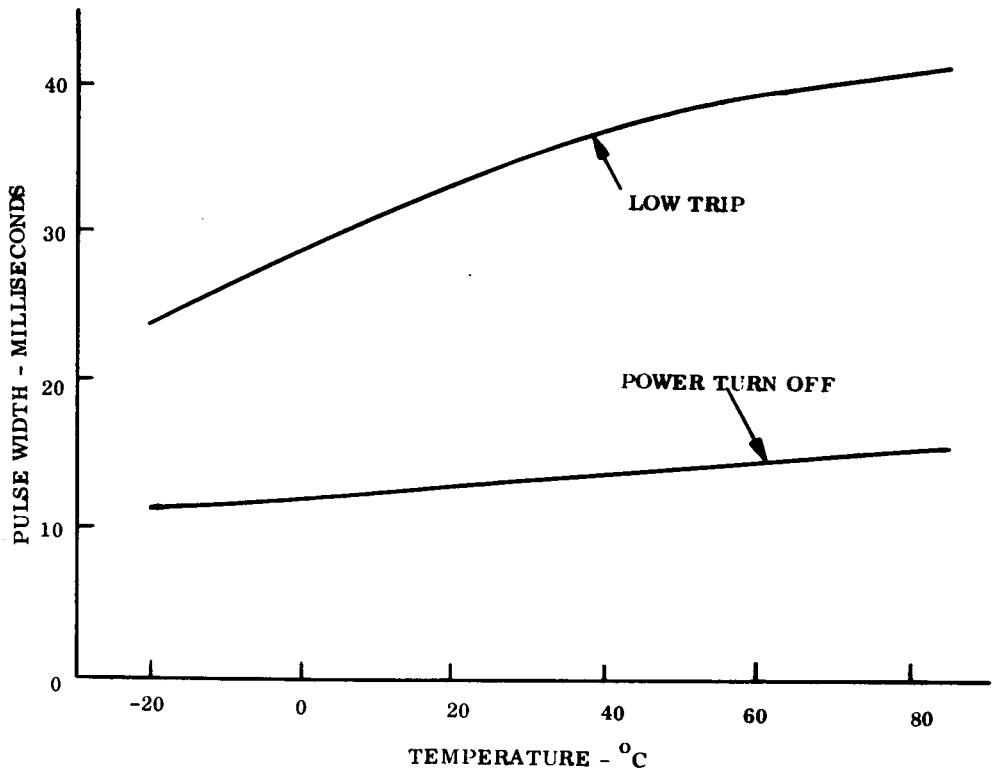


Figure 5.2-9. Current Throttle Steering Switch Output Pulse Width - Qual Unit

The output time delay range of 2.2 to 2.45 milliseconds well exceeds the 1 to 5 millisecond allowed range. Figure 5.2-9 presents the output pulse duration for low trip and power turn off. It can be determined from the photographs that the low temperature pulse duration for power turnoff is being determined by the energy storage capacitor. Since the test results are quite close to the desired 10 milliseconds, an increase of 20% was deemed desirable for the flight energy storage capacitor.

In addition to the changes in design for the flight unit indicated above, higher voltage transistors should be used as indicated on the schematic to preclude failure of the command circuits in the event that a double failure or test condition results in this circuit seeing the unloaded RTG voltage (50-60 Volts) for longer than a transient condition.

5.2.4 FAILURE MODE, EFFECT, AND CRITICALITY ANALYSIS

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.2-1. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	R1	Resistor	Part of input voltage sense divider for undervoltage	Open		Causes inverting input to Op Amp to go low.	Causes switch to select standby current throttle.	Switch can be commanded to initial position.	Not considered a system failure. Power S/S operates the same with either throttle.
2	R2	Resistor	Part of input voltage sense divider for undervoltage.	Open		Causes inverting input to Op Amp to go high.	Steering switch will only work if the PB voltage goes high.		For the PB voltage to go low the CT must fail first and this would constitute the second failure.
3	R3	Resistor	Part of input voltage sense divider for over voltage.	Open		Removes base drive to differential amp Q1-A	Steering switch won't detect an overvoltage on the PB		For the PB voltage to go high, the CT must fail first and this would constitute the second failure.
4	R4	Resistor	Part of input voltage sense divider for over voltage.	Open		Causes Q1 - A to turn on. This pulls down the inverting input to the Op Amp.	Causes steering switch to select standby current throttle	Switch can be commanded to initial position.	Not considered a system failure. Power S/S operates the same with either throttle.
5	R5	Resistor	Q1 - B current limiting resistor	Open		Voltage drop across R6 decreases as Q1 - B shuts off. Q1 - A turns on when emitter voltage drops below base.	Causes invertering input of Op Amp to go low which trips the steering switch to the standby C.T.	Switch can be commanded to initial position.	Not considered a system failure. Power S/S operates the same with either throttle.

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
6	R6	Resistor	Bias emitter voltage of Dif. Amp Q1	Open		Dif. Amp becomes inoperable.	Steering switch will not detect an over-voltage on the PB		For the PB voltage to go high, the CT must fail first and this would constitute the second failure.
7	R7	Resistor	Limits current to voltage refer ence.	Open		Non-inverting input to Op Amp goes low.	Steering switch will not detect either high or low PB voltage.		Complete wipe-out of PB.
8	R8	Resistor	Limits current to non-invert-ing input of Op Amp.	Open		Non-inverting input to Op Amp goes low.	Steering switch will not detect either high or low PB voltage.		Complete wipe-out of PB.
9	R9	Resistor	Limits charging current for C3	Open		Power to Op Amp and relay would be lost	Steering switch will not operate, nor can it be commanded to select the standby C.T.		Complete wipe-out of PB.
10	R10	Resistor	Feedback which deter-mines the reset level for an under voltage trip condition	Open		No hysteresis. Oscillation of Op Amp could occur if undervoltage level was right at the trip point	In this case, its possible the steer-ing switch would not select the standby C.T.		
11	R11	Resistor	Feedback which deter-mines the reset level for an over-voltage trip condition	Open		No hysteresis. Oscillation of Op Amp could occur if overvoltage level was right at the trip point.	In this case, its possible the steer-ing switch would not select the standby C.T.		

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
12	R12	Resistor	In conjunction with C1, determines command duration to the relay switch.	Open		Loss of control of the relay switch by the failure detection circuits	Steering switch won't operate if the P.B. voltage goes low or high		Complete wipe out of P.B.
13	R13	Resistor	Provides discharge path to time delay capacitor C2	Open		C2 would not completely discharge. Would reduce the time delay of the Op Amp output.	Would increase the transient susceptability of the steering switch. Could cause transfer to standby C.T.	NONE	
14	R14	Resistor	Q2 leakage resistor	Open		Q2 could turn on if leakage current was high.	Transfers to the standby C.T.		
15	R15	Resistor	Q3 leakage resistor	Open		Q3 could turn on if leakage current was high.	Transfers to the standby C.T.		

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
16	R16	Resistor	Limits Q2 collector current	Open		Loss of drive to Q3.	The standby C.T. can't be selected by either the detection circuit or by CCS command if P.B. voltage goes low or high	NONE	Complete wipe-out of P.B.
17	R17	Resistor	Current limits the CCS command to the steering switch	Open		Loss of drive to Q2 by command only	The standby C.T. can't be selected by CCS command	Automatic control still remains.	
18	R18	Resistor	Current limits the reset command to the steering switch	Open		Loss of drive to Q5.	CCS can't command the steering switch to return to the first C.T.		There should be no reason to return to the first CT in flight.
19	R19	Resistor	Limits Q4 collector current	Open		Loss of drive to Q5.	CCS can't command the steering switch to return to the first C.T.		There should be no reason to return to the first CT in flight.
20	R20	Resistor	Q5 leakage resistor	Open		Q5 could turn on if leakage current was high.	The reset coil of K1 would remain energized thus prohibiting transfer to the standby C.T.		Complete wipe-out of P.B.
21	CR1	Diode	Prohibits energy storage capacitor C3 from discharging into the Dif Amp. circuit and into an undervoltage P.B.	Open		Power to most of the steering switch would be lost.	No possible transfer to the standby C.T.	The diode is parallel redundant to reduce this possibility	Failure effect is if both diodes fail open.

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
21				Short		Energy storage capacitor C3 would discharge into Dif. Amp and under-voltage P.B.	If the P.B. voltage goes low enough, its possible there won't be sufficient energy to transfer the steering switch relay.		Potential wipe-out of P.B.
22	CR2	Zener Diode	Voltage reference for both the Op Amp and Dif. Amp.	Open		Op Amp non-inverting input goes high while Dif Amp action causes Op Amp inverting input to go low.	Transfer to stand-by C.T.	Output of Op Amp is capacitively coupled. Failure is nonrepetitive. Can be overridden by CCS if failure can be identified.	
				Short		Op Amp non-inverting input goes low while Dif Amp action causes Op Amp inverting input to go even lower.	Transfer to stand-by C.T.	Output of Op Amp is capacitively coupled. Failure is nonrepetitive. Can be overridden by CCS if failure can be identified.	

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
23	CR3	Zener Diode	Minimum Op Amp output voltage would not allow Q2 to cut off. This zener voltage drop compensates for that.	Open		Isolates Op Amp output from transistor Q2.	Steering switch won't operate if the P.B. voltage goes low or high.		Complete wipe-out of P.B.
				Short		Decreases sensitivity such that Op Amp output only increases .7V to turn on Q2.	Possible transfer standby C.T. due to noise.		
24	CR4	Diode	Provides isolation from the CCS command source	Open		Can't turn on Q2 from the CCS command source.	Can't command the steering switch to select the standby C.T.	Still have the automatic capability.	
				Short		Loss of transient immunity	Transient on command line might turn on Q2 which transfers the steering switch to the standby C.T.	Can be returned to first C.T. if failure can be identified.	
25	CR5	Diode	Prevents back biasing base-emitter of Q2 when capacitor C1 discharges	Open		Reverse bias will burn out Q2 - K1 set coil can't be energized again. (Q2 BV_{ebo} = 6 V at I_e = 10μA)	None. For the capacitor to discharge and cause this Q2 damage; it must have first been charged by the Op Amp which would transfer the steering switch to the standby C.T.		When the standby C.T. is selected, the system would not return to the first C.T.
				Short		None - Diode is series redundant	NONE		

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
26	CR6	Diode	Relay coil transient suppression	Open		Current spike on DC line when Q3 shuts off.	Could cause interference with other circuits.		
				Short		K1 set coil could not be energized	No transfer by steering switch to standby C.T. if P.B. voltage goes low or high		Complete wipe-out of P.B.
27	CR7	Diode	Relay coil transient suppression	Open		Current spikes on DC line when Q5 shuts off.	Could cause interference with other circuits.		
				Short		K1 reset coil could not be energized.	Can't command the return to the first C.T.		Probability wouldn't do this in flight any way.
28	C1	Capacitor	A.C. couple the Op Amp output to the control relay coil	Open		Loss of control of the relay switch by the failure detection circuits	Steering switch won't operate if the P.B. voltage goes low or high	Can be commanded by CCS to select standby C.T.	Complete wipe-out of P.B.
				Short		No effect unless other parts fail which cause the OP Amp to go high.	NONE		
29	C2	Capacitor	Provide a time delay of Op Amp output for transient immunity	Open		No delay	A transient could cause transfer to the standby C.T.	Can be returned to the first C.T. by CCS command if failure can be identified.	
				Short		Op Amp output will be grounded	Steering switch won't operate if the PB voltage goes low or high.		Complete wipe-out of P.B.

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
30	C3	Capacitor	Energy storage	Open		If P.B. voltage goes very low, the Op Amp and relay would not have sufficient voltage to operate	No transfer to the standby C.T. if the P.B. voltage goes low.		
				Short		Power distribution in R9 increases to 15 watts. Resistor would fail open.	Loss of steering switch. No transfer to standby current throttle.		Complete wipe-out of P.B.
31	LM108	Operational Amplifier	Compares the P.B. voltage level with a reference to determine a failure condition.	Output High		Provides drive to to Q2	Immediately transfers the steering switch to the standby C.T.		
				Output Low		Loss of drive to Q2 at time of failure.	Steering switch won't select the standby C.T. if P.B. voltage goes low or high.		Complete wipe-out of P.B.
32	Q1	Transistor	Differential Amplifier which detects a high voltage on the P.B.	Open		If Q1 - A fails, a high voltage on the P.B. will not be detected. If Q1 - B fails, Q1 - A turns on. Pulls down the inverting input to the Op Amp.	Steering switch won't select the standby C.T. if P.B. voltage goes high. Steering switch immediately transfers to standby C.T.		

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
32				Short		If Q1 - A fails, it pulls down the inverting input to the Op Amp.	Steering switch immediately transfers to standby C.T.		
						If Q1 - B fails, a high voltage on the P.B. will not be detected	Steering switch won't select the standby C.T. if P.B. voltage goes high.		
33	Q2	Transistor	Amplification of Op Amp and CCS command signal	Open		Can't turn on Q3 and K1 set coil.	Steering switch won't select the standby C.T.		Complete wipe-out of P.B.
				Short		Q3 and K1 set coil will be energized.	Steering switch will transfer to standby C.T.		
34	Q3	Transistor	Amplification of Q2 signal. Drives K1 set coil	Open		Can't turn on Q3 and K1 set coil.	Steering switch won't select the standby C.T.		Complete wipe-out of P.B.
				Short		Q3 and K1 set coil will be energized.	Steering switch will transfer to standby C.T.		
35	Q4	Transistor	Amplification of CCS command which returns steering switch to first C.T.	Open		Can't turn on Q5 and K1 reset coil	Steering switch can't be returned to first C.T.		Probably won't be used in flight any way.
				Short		Q5 and K1 reset coil will be energized.	Steering switch can't transfer to the standby C.T. when required.		Complete wipe-out of P.B.

Table 5.2-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component STEERING SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
36	Q5	Transistor	Amplification of Q4 signal. Drives K1 reset coil.	Open		Can't turn on Q5 and K1 reset coil	Steering switch can't be returned to first C.T.		Probably won't be used in flight any way.
				Short		Q5 and K1 reset coil will be energized.	Steering switch can't transfer to the standby C.T. when required.		Complete wipe-out of P.B.
37	K1	Relay (Mag-Latch. Normally reset.)	Reset-First C.T. on	Fails to make reset contact		Can't select first C.T.	See remarks		Probably won't be used in flight Steering switch is placed in this position prior to flight.
			Set - Stand-by C.T. on.	Fails to make set contact		Can't select standby C.T.	If the standby C.T. is required due to the failure of the first C.T., the P.B. would be lost.		The LVCO must be relied on to clear spacecraft load faults.

5.3 SHUNT REGULATOR

5.3.1 FUNCTIONAL REQUIREMENTS

The shunt regulator assembly regulates the spacecraft main bus voltage such that the electrical power drawn from the RTG power source is relatively constant. This permits operation of the RTG at a practically constant voltage near its maximum power point. The main bus is regulated to 30 volts dc $\pm$ 1 percent by remote voltage sensing this bus and shunting the appropriate amount of current to maintain the voltage within the allowable range. This regulation takes place over all combinations of load variation, input line variation, temperature variation and long term drift.

5.3.2 DESIGN DESCRIPTION (FIGURE 5.3-1)

The overriding design criteria for the shunt regulator is that no single failure degrades the overall operation in any manner. This goal is satisfied by a quad-redundant configuration. Each of the four regulators (Figure 5.3-2) is composed of four sequenced stages which are serially operated as the load demand decreases and the corresponding shunted current increases. A detailed schematic of one regulator of the quad is shown in Figure 5.3-3.

As the load demand decreases and the bus voltage begins to rise above the trip level set by the select-by-test resistor in the reference of the error amplifier- A1, the output of A1 rises to turn on transistor-Q53 which drives the base of transistor-Q54, the control element of the Zener diode sequencing logic. As Q54 initially turns on, it begins to drive transistor-Q1 which is the driver of the shunting transistors of the first sequence. Which transistor of the three parallel transistors-Q5, Q6, Q7 turns on first is controlled by the characteristics of the transistor. That transistor with the lowest V_{BE} will turn on first. Once one of the three has turned on, however, the negative feedback caused by the resistor in the emitter of the transistor causes the others to turn on and consequently share the shunted current equally. As the load demand continues to decrease, the output of A1 continues to rise which ultimately causes the voltage at the emitter of Q54 to rise. When the voltage reaches 3.3 volts, the second sequence turns on; when the voltage reaches 6.2 volts, the third sequence turns on; when the voltage reaches 9.1 volts, the fourth sequence turns on. Each of last three sequences is identical in

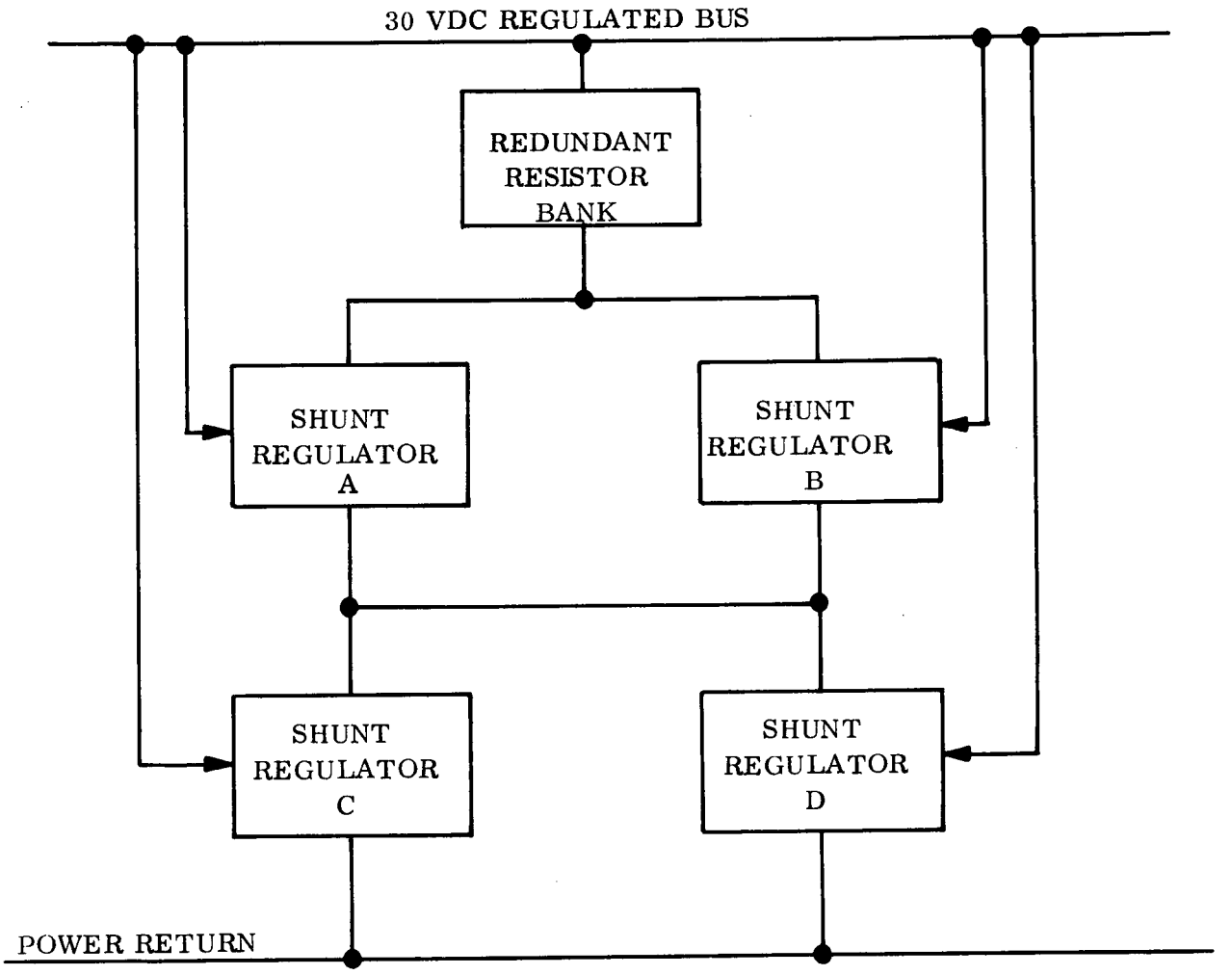


Figure 5.3-1. Shunt Regulator Block Diagram

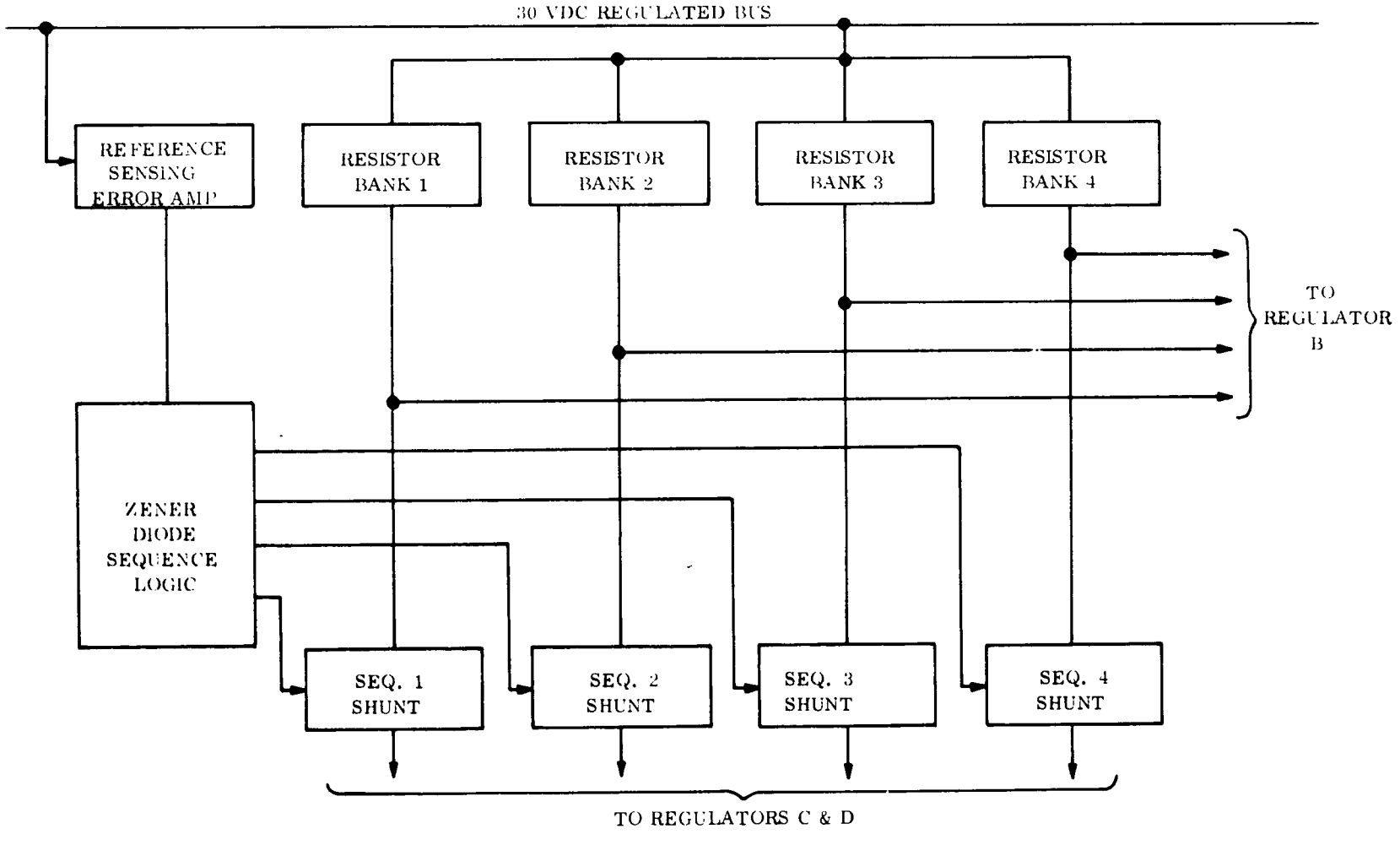


Figure 5.3-2. Shunt Regulator A Block Diagram

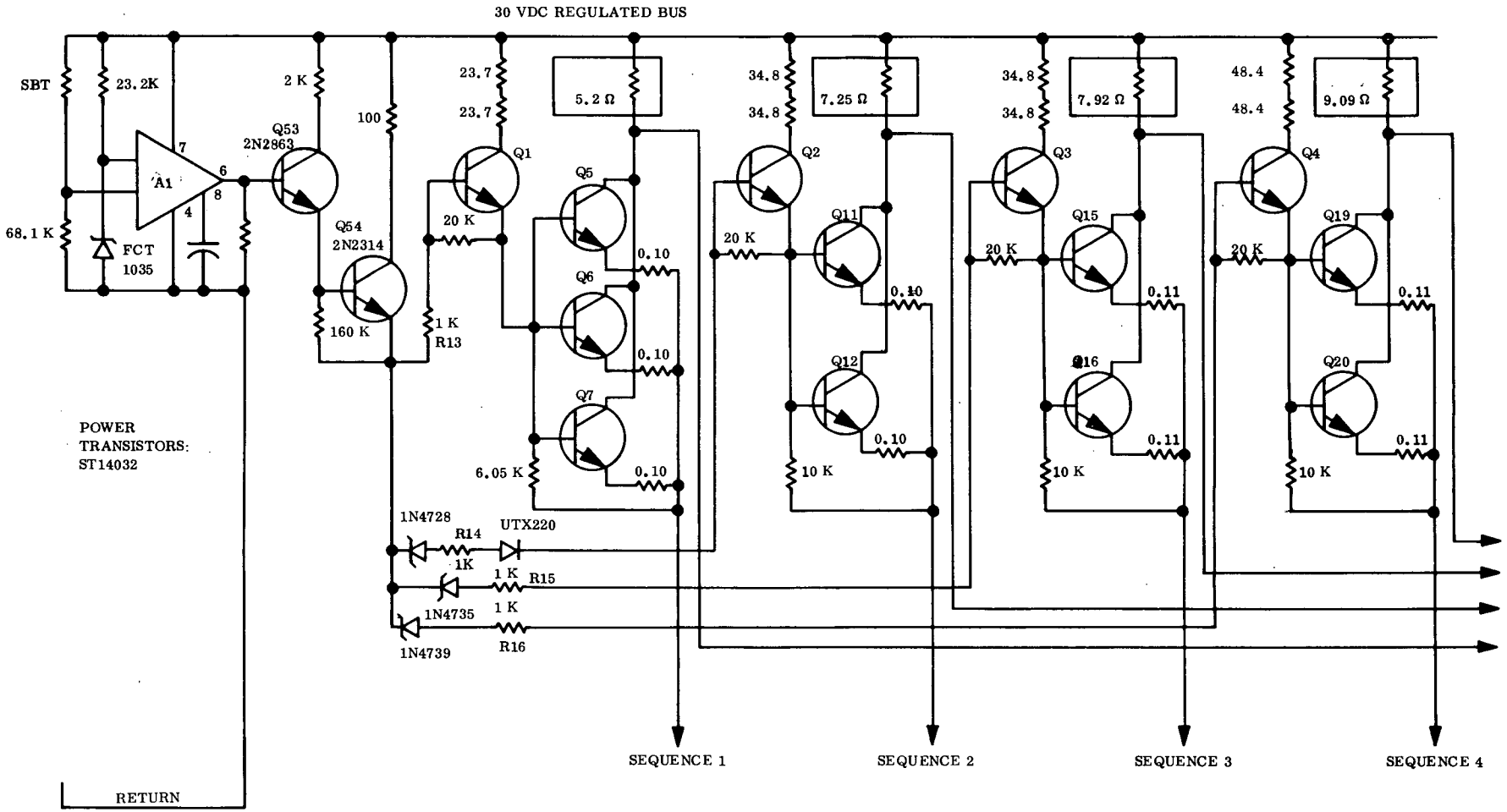


Figure 5.3-3. One of Four Sequenced Shunt Regulators

theory of operation to the first except for the fact that it contains two parallel shunting transistors, instead of three, for a corresponding reduced shunt power capability. Each of the other three regulators of the quad-redundant configuration is identical in design to that shown in Figure 5.3-3. Due to the high gain of the operational amplifier and the discrete values available for setting the regulation point for each op amp, the precise points of regulation for each regulator in the quad do not overlap. The particular regulator in the quad which turns on first is a function of the characteristics of the op amp, its reference voltage, and the sample of the main bus provided by its voltage divider. Once a particular sequence is regulating however, one regulator in either the upper or lower half of the quad will be operating in the linear region while the regulator in parallel is off. The two regulators in the corresponding alternate half will be either one off and the other saturated or both in a saturated mode. When a particular sequence's shunt capability is reached and it saturates, the next sequence begins operation. The criteria controlling which half will be operating and which half will be saturated is identical to that of the previous sequence and consequently arbitrarily controlled by internal piece part characteristics. This operation continues until the full 720 watt capability of the shunt is exceeded and the shunt can no longer regulate.

The gains of the power transistors vary from 17.5 to 29.0 depending on the particular sequence and mode of operation. Using a gain of 25 for the power transistors, 0.9 volts for V_{BE}, and 10 volts to turn on all four sequences via the zener diode logic, less than a 21 volt output of the op amp will produce near saturation of all four sequences. Therefore, using the typical large signal voltage gain of the op amp of 300 volts/millivolt, and a 1:5 voltage sense divider, the bus voltage swing required to provide zero to maximum shunting is merely 0.35 millivolts. This is the reason for the extremely tight regulation versus load ability of the shunt regulator. The variation in regulation occurs only as a function of temperature.

To illustrate the shunt regulator's inherent protection against single piece part failure modes consider the case if one of the transistors of a quad were to fail open, its particular parallel partner (or partners, in the case of the first sequence) in that section of the quad can still shunt the necessary current and remain operating in the required derated region. If the transistor were to fail short, that section of the quad would be lost. Then the section in parallel would operate in a saturated mode while one of the sections in other half of the quad would control in the linear region.

5.3.3 TEST RESULTS

The RTG was simulated by two 30 volt power supplies, connected in series, with an in line 1.5Ω resistor to simulate beginning of mission source characteristics. Steady state voltages were measured with a digital voltmeter, Hewlett-Packard model 3460B. Currents were measured with Weston Portable Standard Ammeter, Model 931. Transient and ac voltages were measured on a Tektronix oscilloscope, Model 545B, using type 533 and CA preamps. ac currents were measured on the oscilloscope as the voltage across a .005Ω shunt. AC currents for impedance measurements were generated using a McIntosch amplifier, Model ME60, with an isolation transformer and sinusoidal generator.

Regulation of the shunt regulator was tested by measuring the voltage at numerous shunted currents between 1 and 20 amps. Output impedance was measured using the test setup of Figure 5.3-4. A measured, sinusoidal variation in load current is induced and the resulting voltage variation also measured. Transient response was measured with the setup of Figure 5.3-5. A 3.33 amp (100 watt) load was switched on and off while monitoring the bus with the oscilloscope. The test was conducted at 5, 10, and 15 amps shunt current. Standby power was measured by supplying 30 volts input to the unloaded shunt, and measuring the input current. Different sections and sequences of the shunt were disabled or shorted out, and the effect on the voltage observed.

Figure 5.3-6 presents regulation results. As predicted, regulation versus load is immeasurable, and the temperature variation is slight. Tables 5.3-1 through 5.3-3 present the impedance test results. Figure 5.3-7 graphically presents the results. The shunt output impedance is less than 110 milliohms. Figures 5.3-8 and 5.3-9 present the transient response results for loading and unloading respectively. Unloading transients were all less than 120 millivolts and less than .5 milliseconds. The transient time for a magnitude greater than 100 millivolts was less than 100 microseconds. Loading transients were all less than 150 millivolts and less than 350μ seconds. The transient time for a magnitude greater than 100 millivolts was less than 100μ seconds. Due to the extremely good dc regulation characteristics of the shunt, it is very likely that the steady state bus voltage will always be within 29.8 to 30.2 volts dc and that a transient duration which might exceed the spec limits will be very small

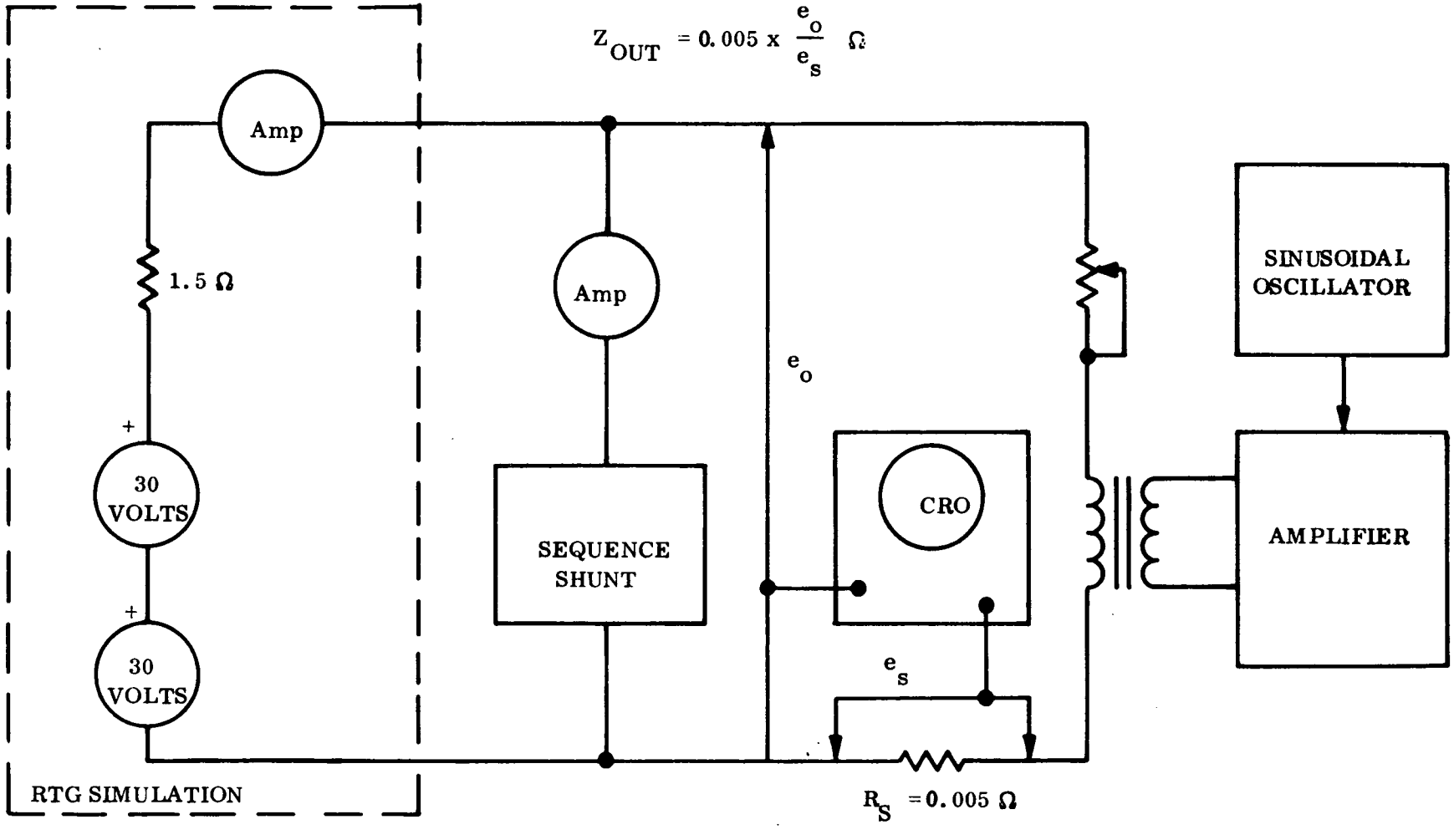


Figure 5.3-4. Output Impedance Test Setup

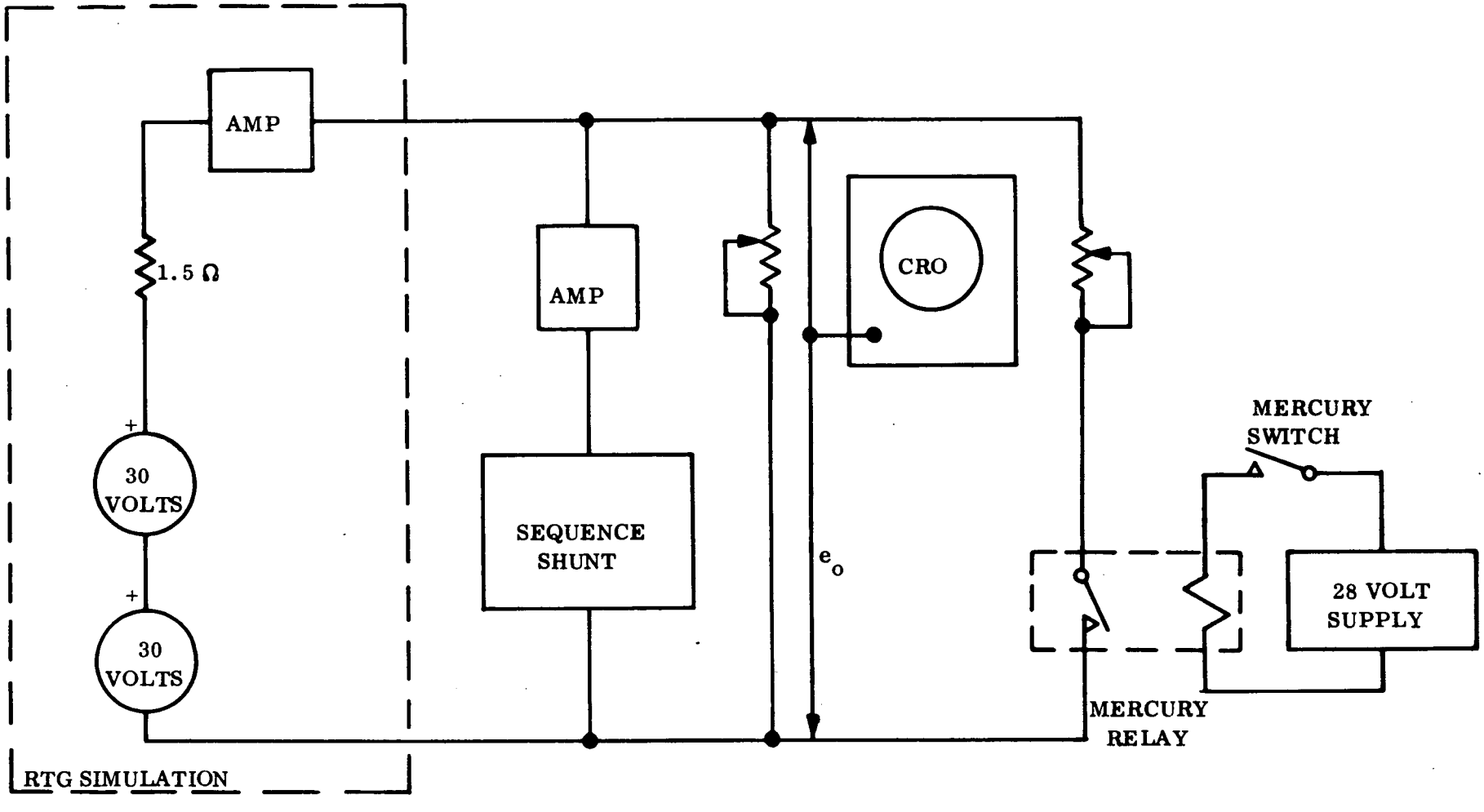


Figure 5.3-5. Transient Test Setup

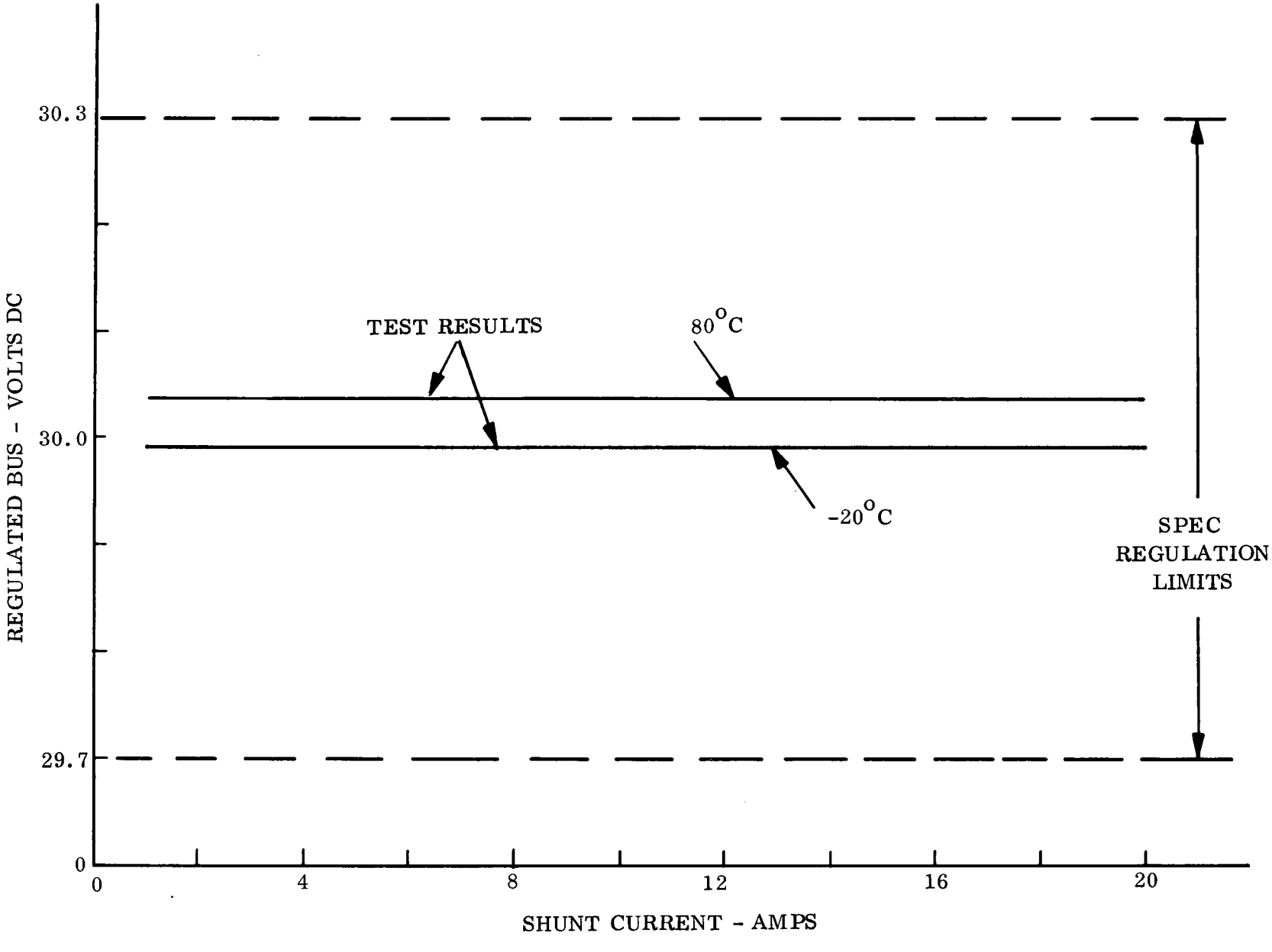


Figure 5.3-6. Sequenced Shunt Regulation Characteristics

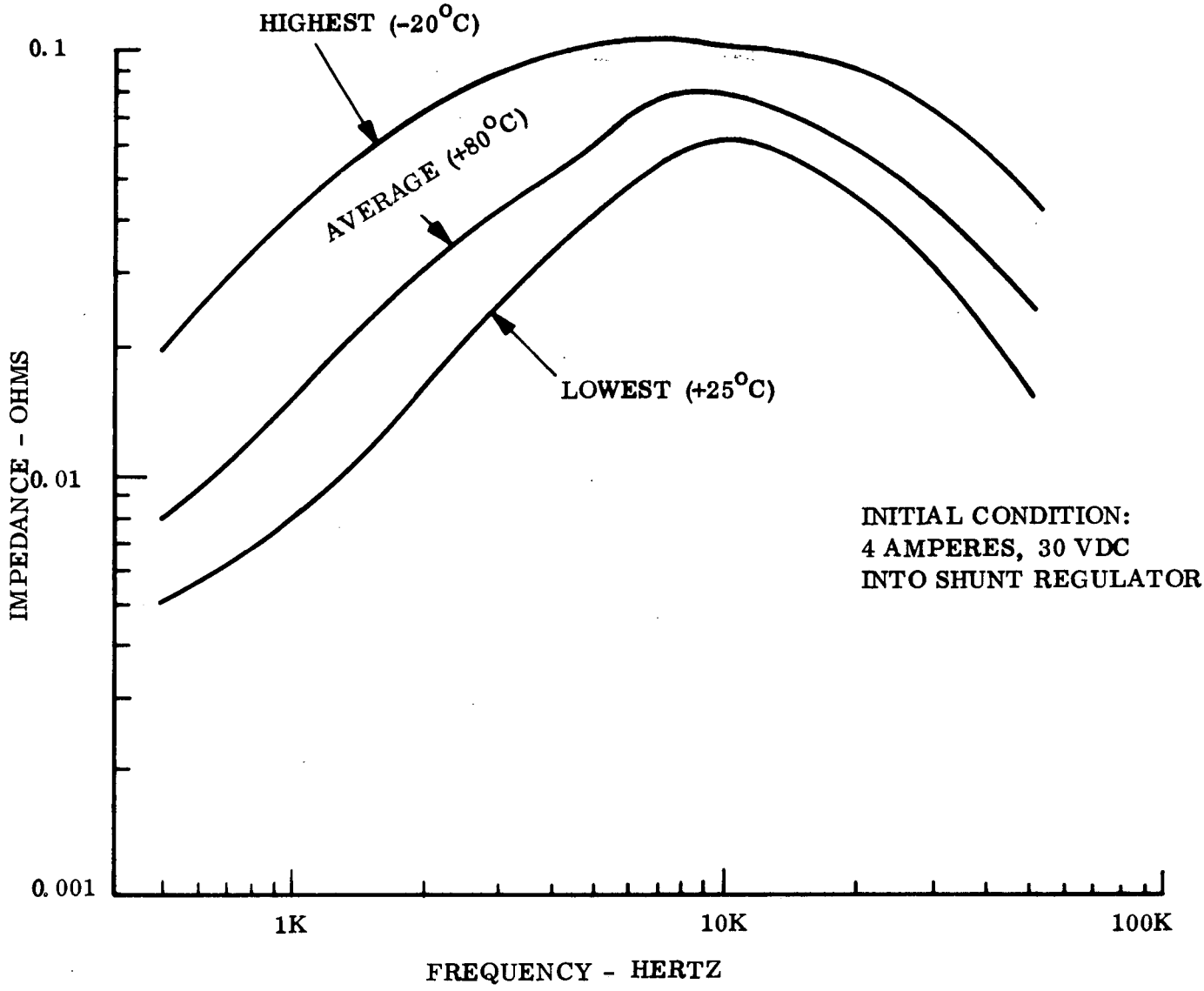
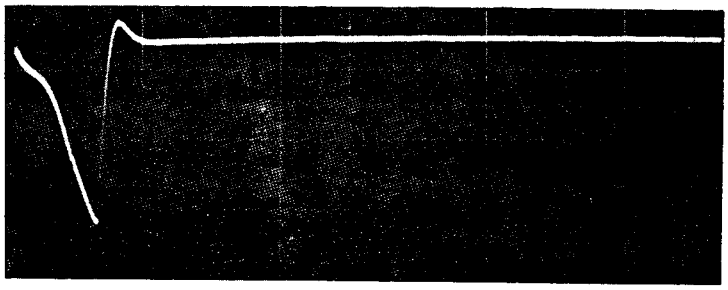
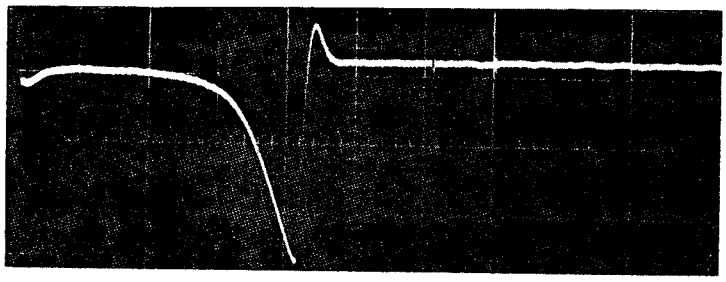


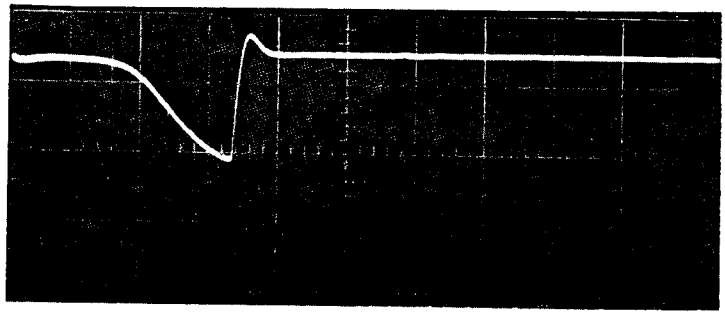
Figure 5.3-7. Sequenced Shunt Regulator Output Impedance Characteristics



LOADING 3.33 A (100w)
I_L = 1.66 A to 5 A
@ I_{SHUNT} = 18.33 A to 15 A
HORIZONTAL = 200 μ sec/cm
VERTICAL = 50 mV/cm

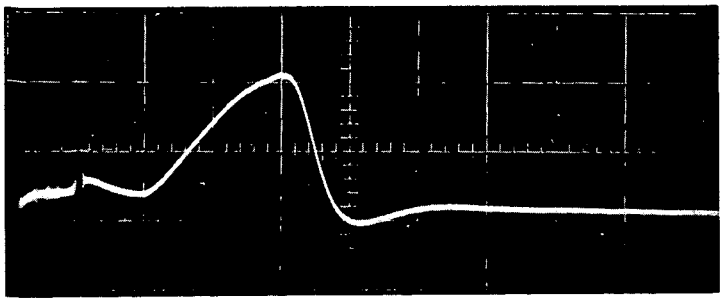


LOADING 3.33 A (100 w)
I_L = 11.66 A to 15 A
@ I_{SHUNT} = 8.33 A to 5.0 A
HORIZONTAL = 200 μ sec/cm
VERTICAL = 20 mV/cm

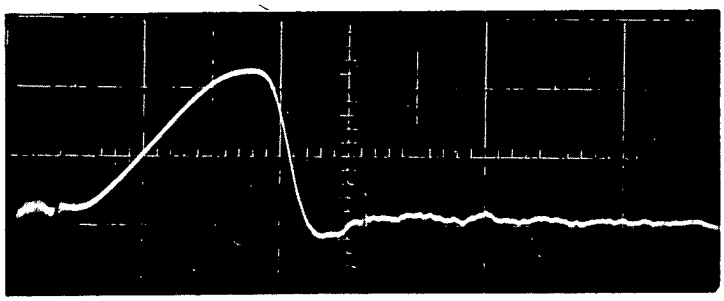


LOADING 3.33 A (100 w)
I_L = 6.66 A to 10 A
@ I_{SHUNT} = 13.33A to 10 A
HORIZONTAL = 200 μsec/cm
VERTICAL = 50 mV/cm

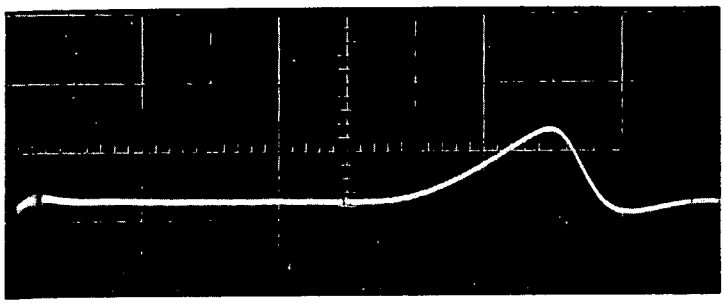
Figure 5.3-8. Sequenced-Shunt Regulator Transient Load Response



UNLOADING 3.33 A (100 w)
I_L = 5 A to 1.66 A
@ I_{SHUNT} = 15 A to 18.33 A
HORIZONTAL = 100 μsec/cm.
VERTICAL = 50 mV/cm



UNLOADING 3.33 A (100 w)
I_L = 10 A to 6.66 A
@ I_{SHUNT} = 10 A to 13.33 A
HORIZONTAL = 100 μsec/cm
VERTICAL = 50 mV/cm



UNLOADING 3.33 A (100 w)
I_L = 15 A to 11.66 A
@ I_{SHUNT} = 5 A to 8.33 A
HORIZONTAL = 100 μsec/cm
VERTICAL = 50 mV/cm

Figure 5.3-9. Sequenced-Shunt Regulator Transient Unload Response

Table 5.3-1. Output Impedance vs. Frequency (+25°C)

SHUNT-AMPS / Freq.-Hz.	4			8			13			16		
	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω
500	14	14	0.005	13	10	0.006	5	4	0.006	9	9	0.005
1000	28	16	0.009	26	10	0.013	10	4	0.012	17	9	0.009
2000	56	16	0.017	52	10	0.026	19	3	0.031	34	8	0.021
5000	100	11	0.045	120	9	0.066	52	4	0.065	85	9	0.047
6000	110	10	0.055	140	8	0.087	52	4	0.065	100	9	0.045
7000	130	10	0.065	155	8	0.098	60	4	0.075	120	10	0.060
10000	130	10	0.065	140	8	0.087	56	4	0.070	140	10	0.070
20000	82	9	0.045	80	7	0.057	36	4	0.045	100	10	0.050
50000	32	9	0.017	30	8	0.018	16	4	0.020	100	11	0.045

Table 5.3-2. Output Impedance vs. Frequency (+80°C)

I_{SHUNT}-AMPS	4			8			13			16		
Freq.-Hz.	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω
500	12	7	0.008	13	10	0.006	7	3	0.011	8	7	0.005
1000	22	7	0.015	24	10	0.012	10	4	0.012	14	8	0.008
2000	39	12	0.016	42	8	0.026	22	3	0.036	28	7	0.020
5000	80	10	0.040	100	7	0.071	48	3	0.080	72	7	0.051
6000	90	10	0.045	100	6	0.083	48	3	0.080	85	7	0.060
7000	105	10	0.052	110	6	0.091	52	3	0.086	100	8	0.062
10000	110	9	0.061	100	6	0.083	46	3	0.076	110	8	0.068
20000	72	7	0.051	56	6	0.046	28	3	0.046	90	9	0.050
50000	24	7	0.017	20	6	0.016	18	3	0.030	36	10	0.018

Table 5.3-3. Output Impedance vs. Frequency (-20°C)

I_{SHUNT}-AMPS	4			8			13			16		
Freq.-Hz.	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω	e_o-mv	e_s-mv	Z_o-Ω
500	8	2	0.020	13	9	0.007	9	7	0.006	7	3	0.011
1000	15	2	0.037	24	4	0.030	14	7	0.010	9	3	0.015
2000	29	2	0.072	42	4	0.052	32	7	0.023	26	4	0.032
5000	40	2	0.100	95	6.5	0.073	52	4	0.065	110	7	0.078
6000	36	2	0.090	110	6	0.091	60	4	0.075	140	8	0.087
7000	34	2	0.085	100	5.5	0.090	70	4.5	0.077	160	7.5	0.106
10000	28	2	0.070	100	5	0.100	80	4	0.100	130	8	0.081
20000	18	1	0.090	56	4	0.070	56	4	0.070	120	9	0.066
50000	7	1	0.035	25	2	0.041	24	5	0.024	60	12	0.025

and always less than 100μ seconds. The volt second spec limit of 50 volt-microseconds (square envelope) was also never exceeded. The maximum unload transient was 37 volt-microseconds, and the maximum loading transient was 39 volt-microseconds. The standby current consumption was measured to be about 3 milliamps which is approximately a 90 milli-watt standby power consumption.

5.3.4 FAILURE MODE, EFFECT, AND CRITICALITY ANALYSIS

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.3-4. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

5.3.4.1 Specific Recommendations

The transient response amplitude and duration can be further reduced by increasing the shunt capacitance.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	R1	Resistor	Part of MB voltage sense divider	Open		Causes decreased voltage on Op Amp A-1 non-inverting input. Output goes low causing entire SR #1 to turn off.		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region.	
2	R2	Resistor	Part of MB voltage sense divider	Open		Causes decreased voltage on Op Amp A-1 non-inverting input. Output goes low causing entire SR #1 to turn off.		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region.	
3	R3	Resistor	Part of MB voltage sense divider	Open		Causes increased voltage on Op Amp A-1 non-inverting input. Output goes high causing entire SR #1 to turn on full.		The resultant decrease in MB voltage causes SR #2 Op Amp A-2 to come from its full on condition into the linear control region.	
4	CR1	Zener Diode	Voltage reference for A-1 Op Amp.	Open		Causes increase in voltage on Op Amp A-1 inverting input. Output goes low causing entire SR #1 to turn off.		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No. _____

Prepared by _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
4				Short		Causes decrease in voltage on Op Amp A-1 inverting input. Output goes high causing entire SR #1 to turn on full.		The resultant decrease in MB voltage causes SR #2 Op Amp A-2 to come from its full on condition into the linear control region.	
5	R4	Resistor limiter for CR1	Current	Open		Causes decrease in voltage on Op Amp A-1 inverting input. Output goes high causing entire SR #1 to turn on full.		The resultant decrease in MB voltage causes SR #2 Op Amp A-2 to come from its full on condition into the linear control region.	
6	A-1	Operational Amplifier	Compares the sampled MB voltage with the zener reference voltage to generate an error signal	High Output		Causes entire SR #1 to turn on full.		The resultant decrease in MB voltage causes SR #2 Op Amp A-2 to come from its full on condition into the linear control region.	
				Low Output		Causes entire SR #1 to turn off.		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
7	C2	Capacitor	Frequency compensation for Op Amp A-1	Open		Op Amp will oscillate			
				Short		Op Amp output will go low causing SR #1 to turn off.		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region	
8	R5	Resistor	Q53 leakage resistor	Open		Q53 could turn on if leakage current was high		The resultant decrease in MB voltage causes SR #2 Op Amp A-2 to come from its full on condition into the linear control region.	Path to ground in Op Amp could provide leakage path for Q53.
9	R6	Resistor	Limits collector current of Q53	Open		Causes entire SR #1 to turn off		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
10	Q53	Transistor	Amplification of the Op Amp output signal	Open		Causes entire SR #1 to turn off.		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region	
				Short		Causes entire SR #1 to turn on full.		The resultant decrease in MB voltage causes SR #2 Op Amp A-2 to come from its full on condition into the linear control region.	
11	Q54	Transistor	Amplification of Q53	Open		Causes entire SR #1 to turn off.		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region	
				Short		Causes entire SR #1 to turn on full.		The resultant decrease in MB voltage causes SR #2 Op Amp A-2 to come from its full on condition into the linear control region	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
12	R187	Resistor	Q54 leakage resistor	Open		Q54 could turn on if leakage current was high		The resultant decrease in MB voltage causes SR #2 Op Amp A-2 to come from its full on condition into the linear control region	
13	R189	Resistor	Limits collector current of Q54	Open		Causes entire SR #1 to turn off.		The resultant increase in MB voltage causes SR #3 Op Amp A-3 to come from its full off condition into the linear control region	
14	R13	Resistor	Limits base drive to Q1 which controls the first sequence of SR #1	Open		Loss of shunting capability of first sequence		Second sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR3 would come on and take over from here.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
15	Q1	Power Transistor	Controls the first sequence of SR #1	Open		Loss of shunting capability of first sequence		Second sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR #3 would come on and take over from here.
				Short		First sequence would remain on.		If that power were required by spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	
16	R191	Resistor	Q1 leakage resistor	Open		Q1 could turn on if leakage current was high. First sequence would remain on.		If that power were required by spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
17	R21	Power Resistor	Limits the current power dissipation in Q1	Open		Loss of shunting capability of first sequence of SR #1		Second sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR #3 would come on and take over from here.
				Short		Increased power dissipation in Q1 could fail transistor.			R21 is backed up by series resistor R22.
18	R22	Power Resistor	Limits the current power dissipation in Q1	Open		Loss of shunting capability of first sequence of SR #1		Second sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR #3 would come on and take over from here.
				Short		Increased power dissipation in Q1 could fail transistor.			R21 is backed up by series resistor R22.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
19	CR2	Zener Diode	Sets the voltage level above sequence #1 at which sequence #2 starts to operate	Open		Loss of shunting capability of the second sequence of SR #1		Third sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR #3 would come on and take over from here.
				Short		Sequence #1 & #2 would overlap. Both would be operating in their linear region simultaneously.	Power dissipation of the shunt regulator in the PCE could go as high as 86 watts (Spec. limit = 50W)		SR #1 can still handle the same amount of power and will be able to maintain bus voltage.
20	R14	Resistor	Limits base drive to Q2 which controls the second sequence of SR #1.	Open		Loss of shunting capability of second sequence		Third sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR #3 would come on and take over from here.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
21	CR17	Diode	CR2 voltage drop is not large enough to keep sequence 1 & 2 from overlapping. The additional drop of this diode is required.	Open		Loss of shunting capability of the second sequence of SR #1		Third sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR #3 would come on and take over from here.
				Short		Sequence #1 & #2 would overlap. Both would be operating in their linear region simultaneously.	Power dissipation of the shunt regulator in the PCE could go as high as 86 watts (Spec. limit = 50W)		SR #1 can still handle the same amount of power and will be able to maintain bus voltage.
22	Q2	Power Transistor	Controls the second sequence of SR #1	Open		Loss of shunting capability of the second sequence		The third sequence would come on to shunt the power	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR 3 would take over from here.
				Short		Second sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on, will turn off to the point where the loads are satisfied.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
23	R192	Resistor	Q2 leakage resistor	Open		Q2 could turn on if leakage current was high. Second sequence would remain on.		If that power was required by the space-craft loads, SR #2 which was full on, will turn off to the point where the loads are satisfied.	
24	R25	Power Resistor	Limits the current - power dissipation in Q2	Open		Loss of shunting capability of the second sequence of SR #1.		Third sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR 3 would come on and take over from here.
				Short		Increased power dissipation in Q2 could fail transistor.			R25 is backed up by R26.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
25	R26	Power Resistor	Limits the current - power dissipation in Q2.	Open		Loss of shunting capability of the second sequence of SR #1.		Third sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR 3 would come on and take over from here.
				Short		Increased power dissipation in Q2 could fail transistor.			R26 is backed up by R25.
26	CR3	Zener Diode	Sets the voltage level above sequence #2 at which sequence #3 starts to operate.	Open		Loss of shunting capability of the third sequence of SR #1		Fourth sequence would come on to shunt the power	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR 3 would come on and take over from here.
				Short		Sequences #1 & #3 would overlap. Both would be operating in their linear region simultaneously.	Power dissipation of the shunt regulator in the PCE could go as high as 84 watts.		SR #1 can still handle the same amount of power and will be able to maintain bus voltage.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No. _____

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
27	R15	Resistor	Limits base drive to Q3 which controls the third sequence of SR #1	Open		Loss of shunting capability of the third sequence.		Fourth sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR 3 would come on and take over from here.
28	Q3	Power Transistor	Controls the third sequence of SR #1	Open		Loss of shunting capability of the third sequence.		Fourth sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR 3 would come on and take over from here.
				Short		Third sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
29	R193	Resistor	Q3 leakage resistor	Open		Q3 could turn on if leakage current was high. Third sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	
30	R29	Power Resistor	Limits the current - power dissipation in Q3	Open		Loss of shunting capability of the third sequence of SR #1.		Fourth sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR 3 would come on and take over from here.
				Short		Increased power dissipation in Q3 could fail transistor.			R29 is backed up by R30.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
31	R30	Power Resistor	Limits the current - power dissipation in Q3.	Open		Loss of shunting capability of the third sequence of SR #1.		Fourth sequence would come on to shunt the power.	Full 600 W shunting capability is still available. SR #1 would continue to control until it could not dissipate any more power. Then SR 3 would come on and take over from here.
				Short		Increased power dissipation in Q3 could fail transistor.			R30 is backed up by R29.
32	CR 4	Zener Diode	Sets the voltage level above sequence #3 at which sequence #4 starts to operate.	Open		Loss of shunting capability of the forth sequence of SR #1.		If additional power must be shunted, SR #3 would come on As the common resistor bank of sequences 1 thru 3 are already dissipating max. power due to SR #1, the output of SR #3 Op Amp would rise to the point where it would turn on sequence #4 to absorb the power.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
32				Short		Sequence #1 & #4 would overlap. Both would be operating in their linear region simultaneously.	Power dissipation of the shunt regulator in the PCE could go as high as 79 watts.		SR #1 can still handle the same amount of power and will be able to maintain bus voltage.
33	R16	Resistor	Limits base drive to Q4 which controls the fourth sequence	Open		Loss of shunting capability of the fourth sequence.		If additional power must be shunted, SR #3 would come on. As the common resistor banks of sequences 1 thru 3 are already dissipating max. power due to SR #1, the output of SR #3 Op Amp would rise to the point where it would turn on sequence #4 to absorb the power.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
34	Q4	Power Transistor	Controls the fourth sequence of SR #1	Open		Loss of shunting capability of the fourth sequence.		If additional power must be shunted, SR #3 would come on. As the common resistor banks of sequences 1 thru 3 are already dissipating max. power due to SR #1, the output of SR #3 Op Amp would rise to the point where it would turn on sequence #4 to absorb the power.	
				Short		Fourth sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	
35	R194	Resistor	Q4 leakage resistor	Open		Q4 could turn on if leakage current was high. Fourth sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
36	R33	Power Resistor	Limits the current power dissipation in Q4	Open		Loss of shunting capability of the fourth sequence of SR #1.		If additional power must be shunted, SR #3 would come on. As the common resistor banks of sequences 1 thru 3 are already dissipating max. power due to SR #1, the output of SR #3 Op Amp would rise to the point where it would turn on sequence #4 to absorb the power.	
				Short		Increased power dissipation in Q4 could fail transistor.			R33 is backed up by R34
37	R34	Power Resistor	Limits the current power dissipation in Q4.	Open		Loss of shunting capability of the fourth sequence of SR #1.		If additional power must be shunted, SR #3 would come on. As the common resistor banks of sequences 1 thru 3 are already dissipating max. power due to SR #1, the output of SR #3 Op Amp would rise to the point where it would turn	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
37								on sequence #4 to absorb the power.	
				Short		Increased power dissipation in Q4 could fail transistor.			R34 is backed up by R33.
38	R37	Power Resistor	Dissipate sufficient power to maintain voltage regulation of the main D.C. Bus.	Open		The first sequence will loose slightly 1/11 of its total power dissipation capability.	The shunt regulator would loose about 15 watts of dissipation capability	Ten remaining parallel paths can dissipate the bulk of the power.	The shunt regulator has more than 600 watt capability. Can accommodate some loss and still meet requirements.
				Short		Peak power dissipation in transistors Q5, Q6, & Q7 will increase from 14 Watts/trans. to 15 Watts/trans.		R38 in series prevents a short from disabling the first sequence resistor bank.	
39	R38	Power Resistor	Dissipate sufficient power to maintain voltage regulation of the main D.C. Bus.	Open		The first sequence will loose slightly 1/11 of its total power dissipation capability.	The shunt regulator would loose about 15 watts of dissipation capability.	Ten remaining parallel paths can dissipate the bulk of the power.	The shunt regulator has more than 600 watt capability. Can accommodate some loss and still meet requirements.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
39				Short		Peak power dissipation in transistors Q5, Q6, & Q7 will increase from 14 Watts/trans. to 15 Watts/trans.		R37 in series prevents a short from disabling the first sequence resistor bank.	
	NOTE:	Resistors R39 thru R58 of the first sequence resistor bank have the same failure modes and effects as R37 and R38 above.							
40	Q5	Power Transistor	Controls the power dissipation to maintain voltage regulation of the Main D.C. Bus.	Open		Peak power dissipation in remaining transistors Q6 & Q7 increases from 14 watts to 21 watts each. Could cause these transistors to fail.		If the first sequence fails open, the second sequence will shunt the power.	
				Short		First sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	
	NOTE:	Transistors Q6 & Q7 have the same failure modes and effects as Q5 above.							

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
41	R59	Resistor	Forces current sharing between power transistors Q5, Q6 & Q7	Open		Peak power dissipation in remaining transistors Q6 & Q7 increases from 14 watts to 21 watts each. Could cause these units to fail.		If the first sequence fails open, the second sequence will shunt the power.	
	NOTE:	Resistors R61 and R63 have the same failure modes and effects as R59 above.							
42	R71	Power Resistor	Dissipate sufficient power to maintain voltage regulation of the Main D.C. Bus.	Open		The second sequence will loose slightly less than 1/9 of its total power dissipation capability.	The shunt regulator would loose about 13 watts of dissipation capability.	Eight remaining parallel paths can dissipate the bulk of the power.	The shunt regulator has more than 600 watt capability. Can accommodate some loss and still meet requirements.
				Short		Peak power dissipation in transistors Q11 & Q12 will increase from 15 watts to 17 watts each.		R72 in series prevents a short from disabling the second sequence resistor bank.	
43	R72	Power Resistor	Dissipate sufficient power to maintain voltage regulation of the Main D.C. Bus.	Open		The second sequence will loose slightly less than 1/9 of its total power dissipation capability.	The shunt regulator would loose about 13 watts of dissipation capability.	Eight remaining parallel paths can dissipate the bulk of the power.	The shunt regulator has more than 600 watt capability. Can accommodate some loss and still meet requirements.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
43				Short		Peak power dissipation in transistors Q11 & Q12 will increase from 15 watts to 17 watts each.		R71 in series prevents a short from disabling the second sequence resistor bank.	
	NOTE:	Resistors R73 and R88 of the second sequence resistor bank have the same failure modes and effects as R71 and R72 above.							
44	Q11	Power Transistor	Control the power dissipation to maintain voltage regulation of the Main D.C. Bus.	Open		Peak power dissipation in the remaining transistor Q12 increases from 15 watts to 30 watts. Could cause this transistor to fail.		If the second sequence fails open, the third sequence will shunt the power.	
				Short		Second sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
45	Q12	Power Transistor	Control the power dissipation to maintain voltage regulation of the Main D.C. Bus	Open		Peak power dissipation in the remaining transistor Q11 increases from 15 watts to 30 watts. Could cause this transistor to fail.		If the second sequence fails open, the third sequence will shunt the power.	
				Short		Second sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	
46	R89	Resistor	Forces current sharing between power transistors Q11 & Q12	Open		Peak power dissipation in remaining transistor Q12 increases from 15 watts to 30 watts. Could cause this transistor to fail.		If the second sequence fails open, the third sequence will shunt the power.	
	NOTE:	Resistor 91 has the same failure modes and effects as R89 above.							

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
47	R98	Power Resistor	Dissipate sufficient power to maintain voltage regulation of the Main D.C. Bus.	Open		The third sequence will loose slightly less than 1/9 of its total power dissipation capability.	The shunt regulator would loose about 12 watts of dissipation capability.	Eight remaining parallel paths can dissipate the bulk of the power.	The shunt regulator has 600 watt capability. Can accommodate some loss and still meet requirements.
				Short		Peak power dissipation in transistors Q15 & Q16 will increase from 13.7 watts to 15.3 watts each.		R98 in series prevents a short from disabling the third sequence resistor bank.	
48	R98	Power Resistor	Dissipate sufficient power to maintain voltage regulation of the Main D.C. Bus.	Open		The third sequence will loose slightly less than 1/9 of its total power dissipation capability.	The shunt regulator would loose about 12 watts of dissipation capability.	Eight remaining parallel paths can dissipate the bulk of the power.	The shunt regulator has 600 watt capability. Can accommodate some loss and still meet requirements.
				Short		Peak power dissipation in transistors Q15 & Q16 will increase from 13.7 watts to 15.3 watts each.		R97 in series prevents a short from disabling the third sequence resistor bank.	
	NOTE:	Resistors R99 thru R114 have the same failure modes and effects as R97 and R98 above.							

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
49	Q15	Power Transistor	Control the power dissipation to maintain voltage regulation of the Main D.C. Bus.	Open		Peak power dissipation in the remaining transistor Q16 increases from 13.7 watts to 27.4 watts. Could cause this transistor to fail.		If the third sequence fails open, the fourth sequence will shunt the power.	
				Short		Third sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	
50	Q16	Power Transistor	Control the power dissipation to maintain voltage regulation of the Main D.C. Bus.	Open		Peak power dissipation in the remaining transistor Q15 increases from 13.7 watts to 27.4 watts. Could cause this transistor to fail.		If the third sequence fails open, the fourth sequence will shunt the power.	
				Short		Third sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
50								to the point where the loads are satisfied.	
51	R115	Resistor	Forces current sharing between power transistors Q15 & Q16	Open		Peak power dissipation in remaining transistor Q16 increases from 13.7 watts to 27.4 watts. Could cause this transistor to fail.		If the third sequence fails open, the fourth sequence will shunt the power.	
	R117 has same failure modes and effects R115.								
52	R123	Power Resistor	Dissipate sufficient power to maintain voltage regulation of the Main D.C. Bus.	Open		The fourth sequence will loose slightly less than 1/9 of its total power dissipation capability.	The shunt regulator would loose about 10 watts of dissipation capability	Eight remaining parallel paths can dissipate the bulk of the power.	The shunt regulator has more than 600 watt capability. Can accommodate some loss and still meet requirements.
				Short		Peak power dissipation in transistors Q19 & Q20 will increase from 12.1 watts to 13.5 watts each.		R124 in series prevents a short from disabling the fourth sequence resistor bank.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
53	R124	Power Resistor	Dissipate sufficient power to maintain voltage regulation of the Main D.C. Bus.	Open		The fourth sequence will loose slightly less than 1/9 of its total power dissipation capability.	The shunt regulator would loose about 10 watts of dissipation capability.	Eight remaining parallel paths can dissipate the bulk of the power.	The shunt regulator has more than 600 watt capability. Can accommodate some loss and still meet requirements.
				Short		Peak power dissipation in transistors Q19 & Q20 will increase from 12.1 watts to 13.5 watts each.		R123 in series prevents a short from disabling the fourth sequence resistor bank.	
	NOTE:	Resistors R125 thru R140 have the same failure modes and effects as R123 and R124 above.							
54	Q19	Power Transistor	Control the power dissipation to maintain voltage regulation of the Main D.C. Bus.	Open		Peak power dissipation in the remaining transistor Q20 increases from 12.1 watts to 24.2 watts. Could cause this transistor to fail.		If the fourth sequence fails open, SR #3 will come on and cause transistors Q21 & Q22 to turn on to control sequence four.	
				Short		The fourth sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
54								to the point where the loads are satisfied.	
55	Q20	Power Transistor	Control the power dissipation to maintain voltage regulation of the Main D.C. Bus.	Open		Peak power dissipation in the remaining transistor Q19 increases from 12.1 watts to 24.2 watts. Could cause this transistor to fail.		If the fourth sequence fails open, SR #3 will come on and cause transistors Q21 & Q22 to turn on to control sequence four.	
				Short		The fourth sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on will turn off to the point where the loads are satisfied.	
56	R141	Resistor	Forces current sharing between power transistors Q19 & Q20	Open		Peak power dissipation in remaining transistor Q20 increases from 12.1 watts to 24.2 watts. Could cause this transistor to fail.		If the fourth sequence fails open, SR #3 will come on and cause transistors Q21 & Q22 to turn on to control sequence four.	

NOTE: R143 has same failure modes as R141.

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
57	R201	Resistor	Leakage resistor for Q5, Q6 & Q7.	Open		Q5, Q6 & Q7 could turn on if leakage current was high. First sequence would remain on.		If that power were required by the space-craft loads, SR #2 which was full on, will turn off, to the point where the loads are satisfied.	
58	R205	Resistor	Leakage resistor for Q11 & Q12	Open		Q11 & Q12 could turn on if leakage current was high. Second sequence would remain on.		If that power were required by the space-craft loads, SR#2 which was full on, will turn off, to the point where the loads are satisfied.	
59	R209	Resistor	Leakage resistor for Q15 & Q16	Open		Q15 & Q16 could turn on if leakage current was high. Third sequence would remain on.		If that power were required by the space-craft loads, SR #2 which was full on, will turn off, to the point where the loads are satisfied.	

Table 5.3-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component SHUNT REGULATOR
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
60	R213	Resistor	Leakage resistor for Q19 & Q20	Open		Q19 & Q20 could turn on if leakage current was high. Fourth sequence would remain on.		If that power were required by the spacecraft loads, SR #2 which was full on, will turn off, to the point where the loads are satisfied.	
61	C1	Capacitor	Improve transient response by lowering the shunt regulator dynamic impedance.	Open		Loss of ½ of the total shunt regulator capacitance.	Increase in recovery time and increase in disturbance amplitude.		
				Short		Causes large current flow thru R187	R187 acts as a fuse and fails open circuit. Will cause an undervoltage until resistor fails.		
	NOTE:	Capacitors C6, C7 & C8 have the same failure modes and effects as C1 above.							
62	R187	Resistor	Acts as a fuse to protect the Main D.C. Bus from a shorted capacitor C1.	Open		Loss of ½ of the total shunt regulator capacitance	Increase in recovery time and increase in disturbance amplitude during Main Bus switching.		
	NOTE:	Resistors R188 thru R190 have the same failure modes and effects as R187 above.							

5.4 MAIN INVERTER

5.4.1 FUNCTIONAL REQUIREMENTS

The main inverter transforms the input voltage of 30 volts dc, ±1 percent from the main bus to 50 volts, rms, +3 percent and -4 percent square-wave. The output power ranges from 145 watts, minimum to 315 watts, maximum. The rise and fall time of the output waveform is 2 ± 1 microseconds. The inverter is designed either to run from a clock synchronized at 4800 Hz or to free run at 4750 Hz + 0 percent and -5 percent. The efficiency is to be at least 92 percent at full load. The output is short circuit protected for a period of 0.5 second with a source capability of 35 amps. The inverter is to operate over a temperature range of $-20^{o}C$ to $+75^{o}C$.

5.4.2 DESIGN DESCRIPTION (FIGURE 5.4-1)

The inverter free run frequency is generated by an operational amplifier oscillator. The basic frequency of operation is determined by an RC time constant (R7-C3). The actual frequency of operation, however, will be determined by the spacecraft central clock. Transistor Q_1 synchronizes the oscillator to the clock frequency.

A buffer amplifier, Q_2, amplifies and squares the oscillator output to drive the bistable multivibrator, Q_3 and Q_4. The state of the multivibrator is changed by the negative going edge of the square wave from the buffer amplifier. Therefore, the output of the multivibrator is a square wave whose frequency is one half the oscillator frequency.

The drive transformer, T_1, converts the high voltage, low current square wave from the multivibrator to a low voltage, high current square wave to drive the power transistors, Q_5 and Q_6. Transformers T_4 and T_5 are volt-second devices which delay the turn on of the off transistor. This notch in the drive waveform allows the on transistor to turn off before the off transistor turns on; thus, preventing both Q_5 and Q_6 from being on at the same time. Resistors R23 and R24 are used to prevent the magnetizing current of the volt-second devices from turning on the output power transistors.

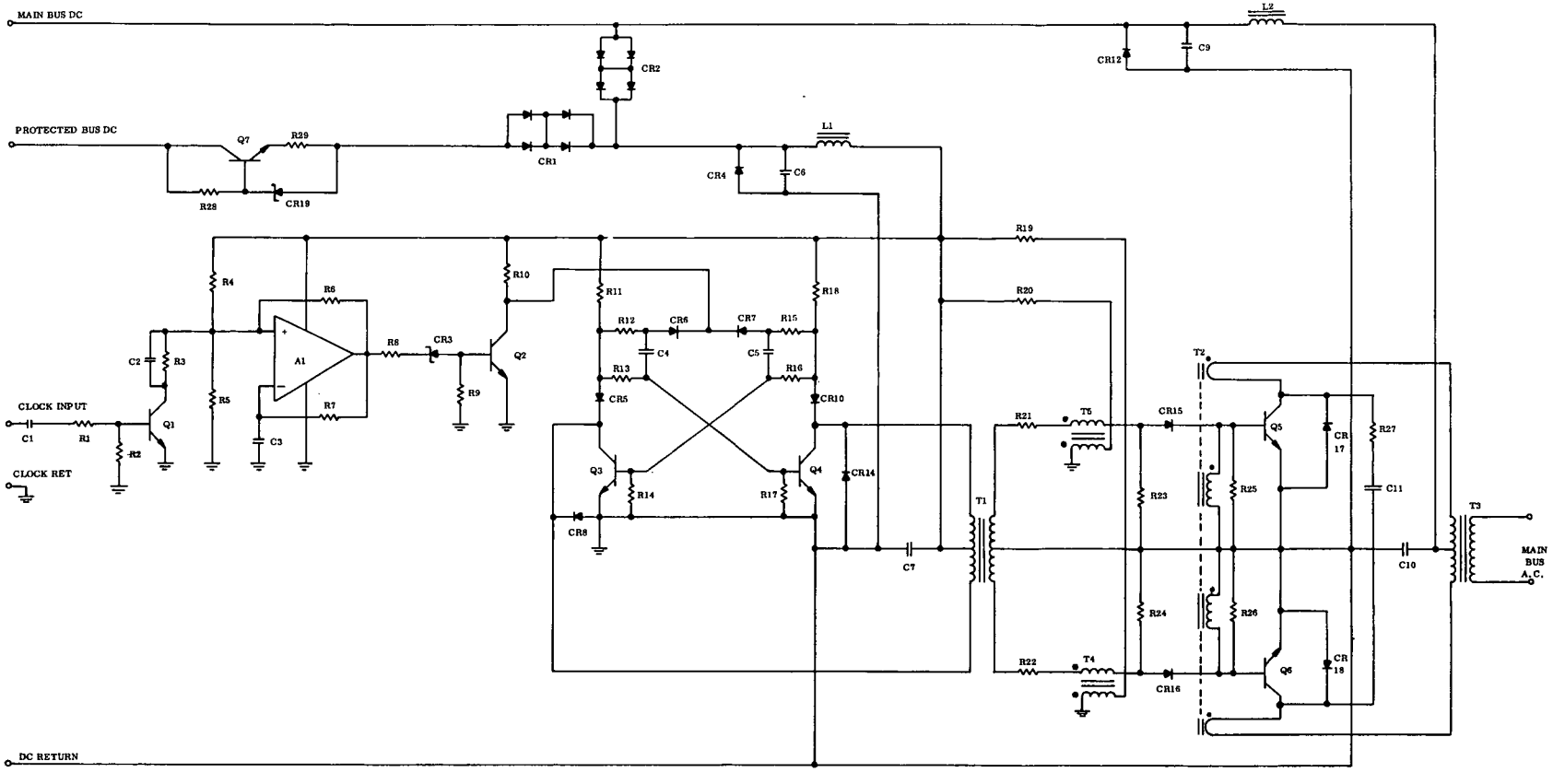


Figure 5.4-1. Main Inverter

Transformer T_2 is a current feedback transformer which increases the base drive as the collector current increases. This allows efficient inverter operation over a wide variation of the load. Resistors R25 and R26 assist in turning off the power transistors.

From the schematic, it is noted that diodes CR_1 and CR_2 couple power from both the main dc bus and the protected dc bus to a common point which powers the oscillator, the multivibrator, the drive transformer, and the volt-second devices. It is also noted that the output power stage is only powered from the main dc bus. This approach was taken because the RTG power source is power limited, and an inverter overload will pull the main dc bus down out of regulation. (A short circuit on the inverter output will draw a maximum of 35 amps, at zero volts, from the power source.) With drive circuitry capable of deriving power from the protected dc bus and current feedback in the output power stage, the inverter can operate into an overload or short circuit.

Since a failure in the oscillator or multivibrator sections could pull both buses out of regulation, a current limiter was placed in series with the protected dc bus line. On the schematic, the limiter is composed of circuit elements, CR_1, R_{28}, R_{29}, and Q_7. Two input filters (L_2, L_2, C_7, C_{10}) reduce the amount of ac ripple current that will appear on the dc buses.

5.4.3 TEST RESULTS

To measure efficiency, the test setup shown in Figure 5.4-2 was used. The input power was calculated from the input voltage and current (P = VI). The output power was calculated from the output voltage and calibrated load resistance ($P = \frac{E^2}{R}$). The inverter efficiency and output voltage versus output power is plotted in Figures 5.4-3, 5.4-4, and 5.4-5. Figure 5.4-3 shows the worst case efficiency which was at an input voltage of 30.3 vdc and a temperature of $+85^{\circ}C$. Figure 5.4-4 shows the nominal efficiency which was at an input voltage of 30.0 vdc and a temperature of $25^{\circ}C$. Figure 5.4-5 shows the best efficiency which was at an input voltage of 29.7 vdc and a temperature of $-20^{\circ}C$. During this testing the free running frequency was also measured. The input voltage and the output power level had no effect on the frequency. However, the frequency varied with temperature from a low of 4600 Hz at $+85^{\circ}C$ to a high of 4644 Hz at $-20^{\circ}C$. This gives a nominal frequency of 4622 Hz $\pm$ 0.5 percent. This is well within the specification of 4750 Hz $^{+0}_{-5}$ percent.

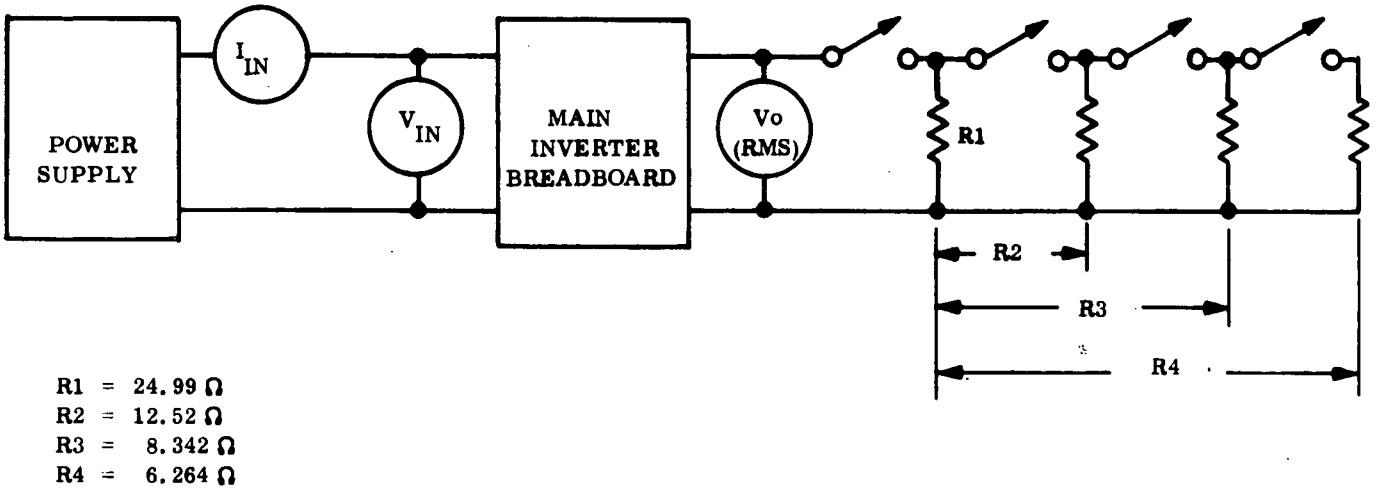


Figure 5.4-2. Efficiency Test Setup

The test setup shown in Figure 5.4-6 was used to test the capability of the inverter to withstand an overload. The load was varied from nominal operating power down to a short circuit, and the input and output voltages and currents were measured. Since the overload voltages and currents are a function of the power source, in this case an RTG simulator, the variations in the data over the temperature range were negligible, less than a total of five percent. Therefore, the nominal cases at a temperature of +25°C are shown. Figure 5.4-7 shows the variation in input and output voltages as a function of output current, and Figure 5.4-8 shows the input current as a function of output current. These two curves definitely show that the inverter can withstand an overload including a shorted output. The reasons the inverter did not draw 35 amps is that cabling losses and diode drops limited the simulator current to 32.4 amps.

From the discussion and curves, it can be concluded that the inverter design meets all of its requirements over a temperature range of -20°C to 85°C and an input range of 30.0 vdc ±1 percent. As can be seen from Figure 5.4-7, the inverter is capable of operating into an overload. In fact, during this testing, the inverter saw a peak output power of 528 watts and the efficiency was still greater than 90 percent.

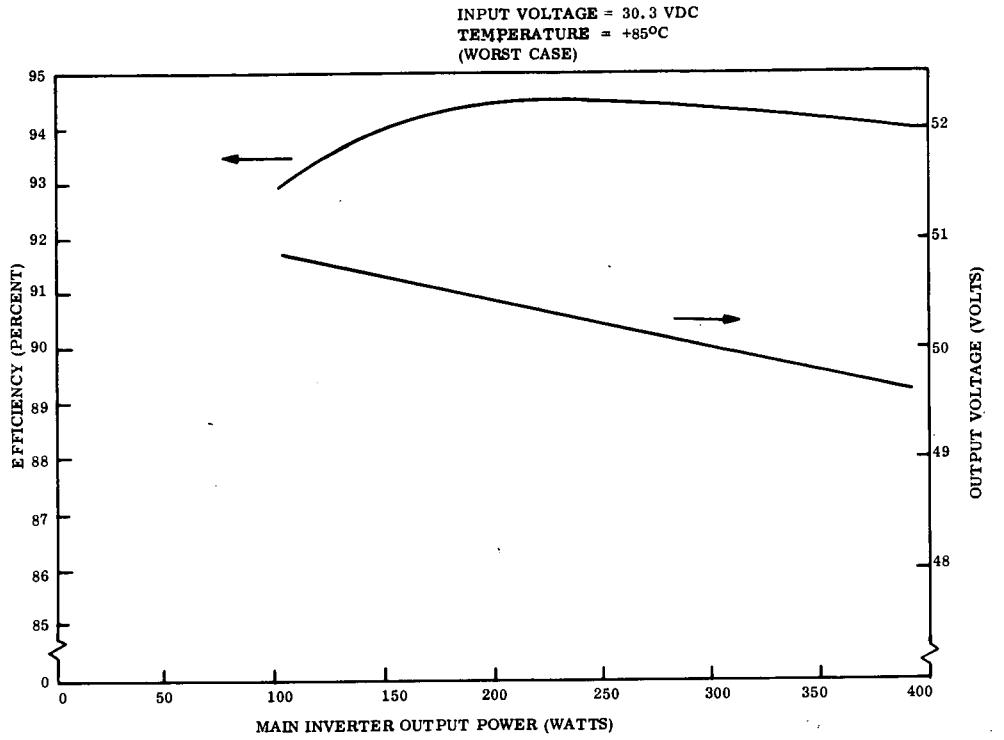


Figure 5.4-3. Efficiency and Output Voltage versus Output Power (Worst Case)

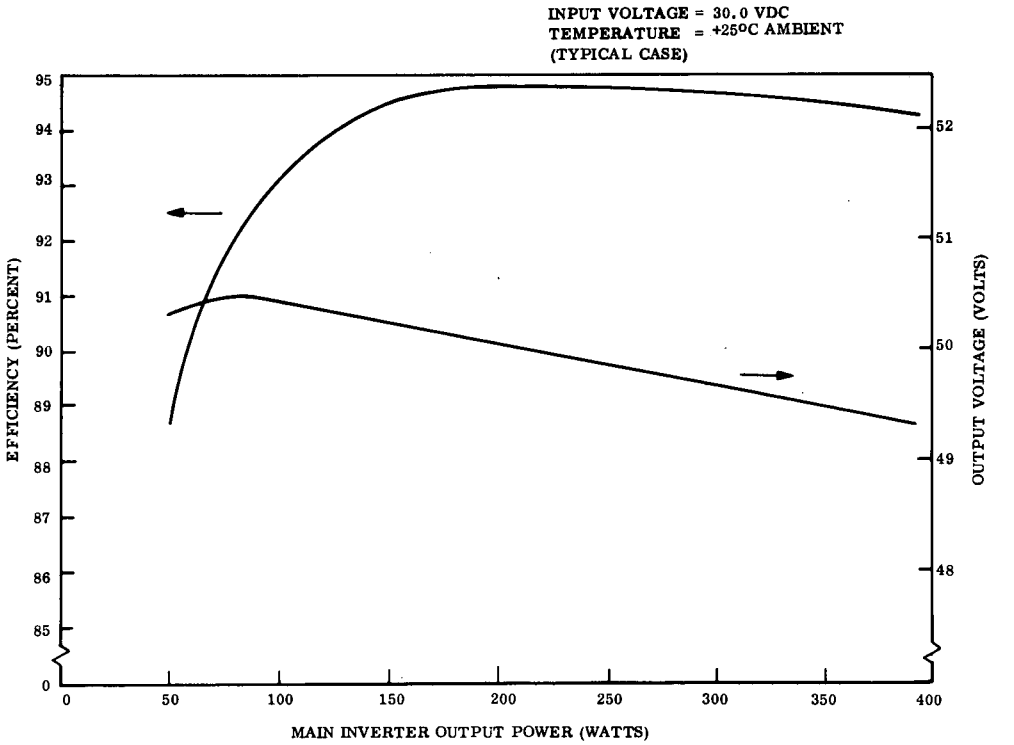


Figure 5.4-4. Efficiency and Output Voltage versus Output Power (Typical Case)

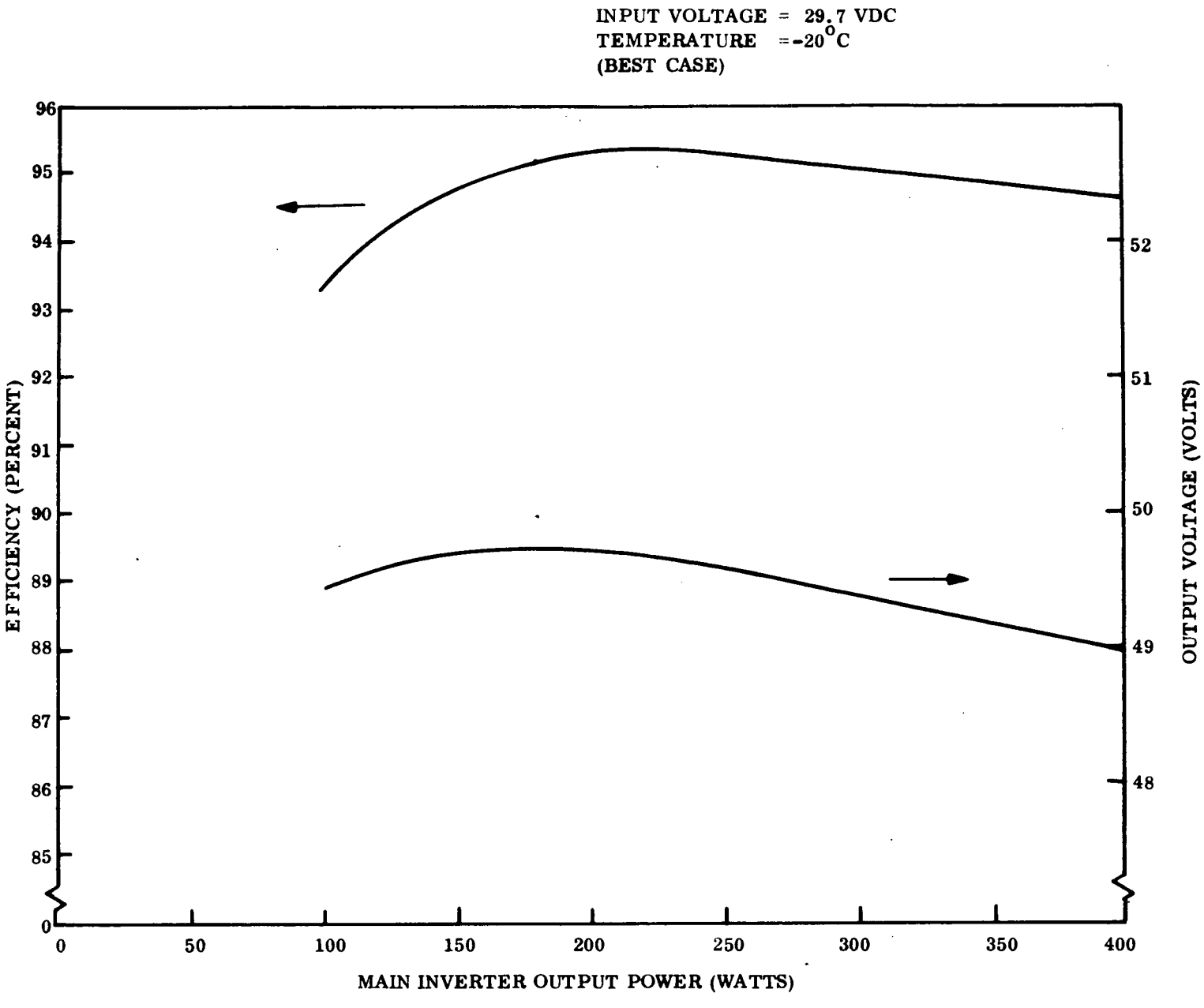


Figure 5.4-5. Efficiency and Output Voltage versus Output Power (Best Case)

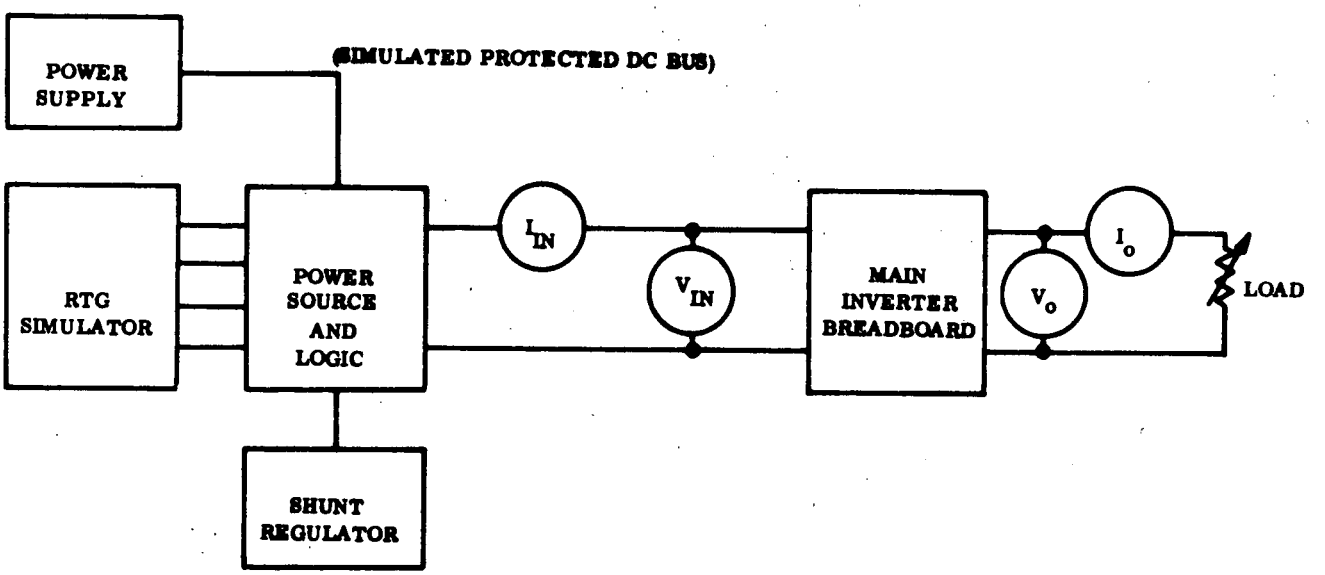


Figure 5.4-6. Inverter Overload Test Setup

5.4.4 FAILURE MODE, EFFECT AND CRITICALITY ANALYSIS

The theory of operation and the functional requirements of the main inverter are identical to the protected bus inverter except for load and output voltage regulation requirements. As the designs are identical, the Failure Mode, Effect and Criticality Analysis performed for the protected bus inverter will apply for the main inverter also.

5.4.4.1 Overvoltage/Undervoltage

The Protected Bus input to the Main Bus Inverter passes through the Main Inverter current limit circuitry. This prohibits a failed Main Bus inverter from overloading the Protected Bus. As the Protected Bus voltage increases, the current through the R29 sense resistor of the current limit circuitry increases to a maximum of 100 milliamperes. At this point, the transistor Q7 comes out of saturation and will drop excessive input voltage to limit the current at this point.

Calculations show that when 100 milliamps are flowing through the current limit circuitry from the Protected Bus, the maximum voltage that can be developed across the switching circuitry is approximately 25 vdc. Therefore, none of the Main Bus Inverter circuitry will be effected by an overvoltage on the Protected Bus.

Undervoltage on the DC input bus caused by an overload on the Main Bus Inverter output will probably not cause failure of the inverter. A quick analysis indicates that at about 14 vdc input, the voltage developed on the T1 secondary is not adequate to provide base drive to Q5 or Q6, and they stop switching. One remains on and the other is off until T2 saturates at which point, both turn off. Because the gain of the transistor at current levels which would cause a bus undervoltage to 14 vdc (18 to 32 amps) is greater than the feedback gain of the T2 transformer, the feedback current into the transistor base is more than adequate to keep the transistor in saturation once it is triggered by the signal from T1. Therefore, the transistor will operate either full on or off and not in the linear region. Other effects of undervoltage are that the LM 101A op amp voltage oscillator is not rated to work below 10 vdc. In addition, when the op amp output drops below about 5 vdc, the zener diode CR 3 no longer conducts and Q2 becomes cutoff. Thus, all switching stops.

It is suggested that the Main and Protected Buses be or'ed together up stream of the current limiter circuit to protect the transistors in the multivibrator during an undervoltage condition (see Protected Bus Inverter discussion).

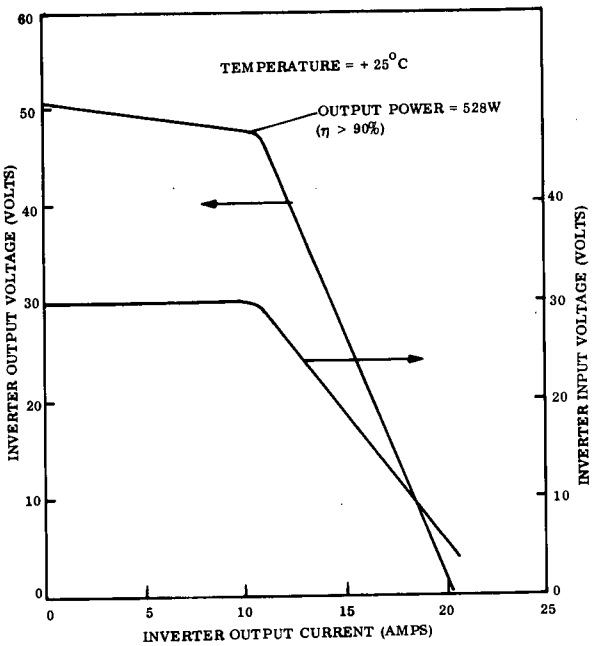


Figure 5.4-7. Inverter Input and Output Voltages versus Output Current (Typical Case)

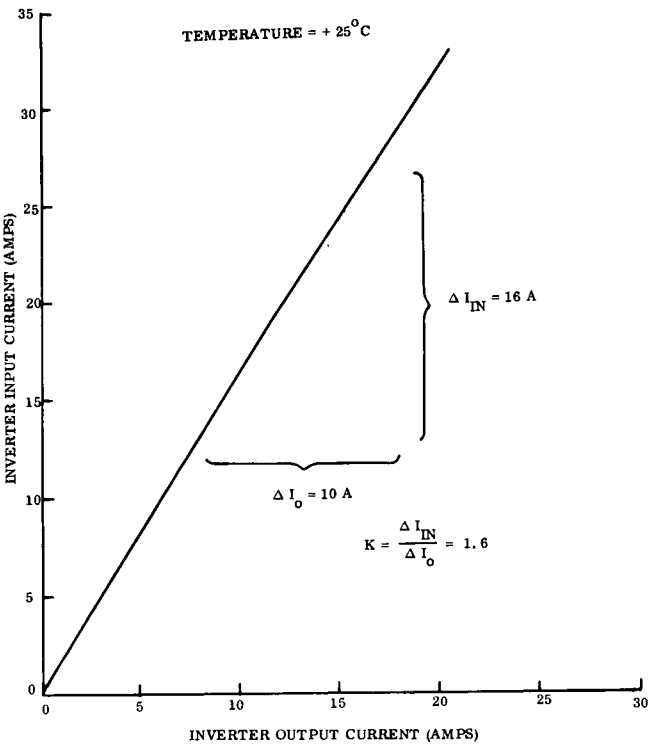


Figure 5.4-8. Inverter Input Current versus Inverter Output Current

5.5 PROTECTED BUS INVERTER

5.5.1 FUNCTIONAL REQUIREMENTS

The protected bus inverter transforms the input voltage of 32.2 volts $\pm$ 0.9 volts, dc, from the protected dc bus to a 50 volt, +5% and -6% RMS square-wave. The output power range is from 45 watts, minimum, to 90 watts maximum with the load being either resistive or at a power factor of 95% lagging. The rise and fall time of the output waveform is 2 $\pm$ 1 microseconds. The inverter is designed either to run from a clock synchronized at 4800 Hz or to free run at 4750 Hz + 0% and -5%. The efficiency is to be at least 92% at full load. The output is short circuit protected for a period of 0.5 seconds with a source capability limited to 11 amperes. The inverter is to operate over a temperature range of -20^{o}C to + 75^{o}C.

5.5.2 DESIGN DESCRIPTION (Figure 5.5-1)

The inverter is composed of a clockpulse amplifier, an oscillator, a bistable multivibrator, a driver amplifier, and a power amplifier. In addition, there is power gating, filtering, and a surge limiter.

5.5.2.1 Clock Pulse Amplifier

While the clock pulses which synchronize the oscillator have not been defined to date, it is assumed that they are of greater than one volt amplitude, positive going, and at least a few microseconds in duration. These pulses are capacitively coupled to the base of transistor Q1, causing momentary conduction in the collector circuit. This provides a momentary dip in voltage at the noninverting input of amplifier A1.

5.5.2.2 Oscillator

The oscillator is composed of operational amplifier A1, positive feedback circuit R7 - C3, and negative feedback circuit R4-R5-R6. The negative feedback stabilizes the amplifier voltage gain at about 1.5. This value provides enough gain for easy oscillation, but a value so low as to provide immunity from external influences, such as open loop amplifier gain variations. The positive feedback causes oscillation at a frequency determined by the values of R4, R5, R6, R7, C3, and little else. These components are chosen so that a frequency

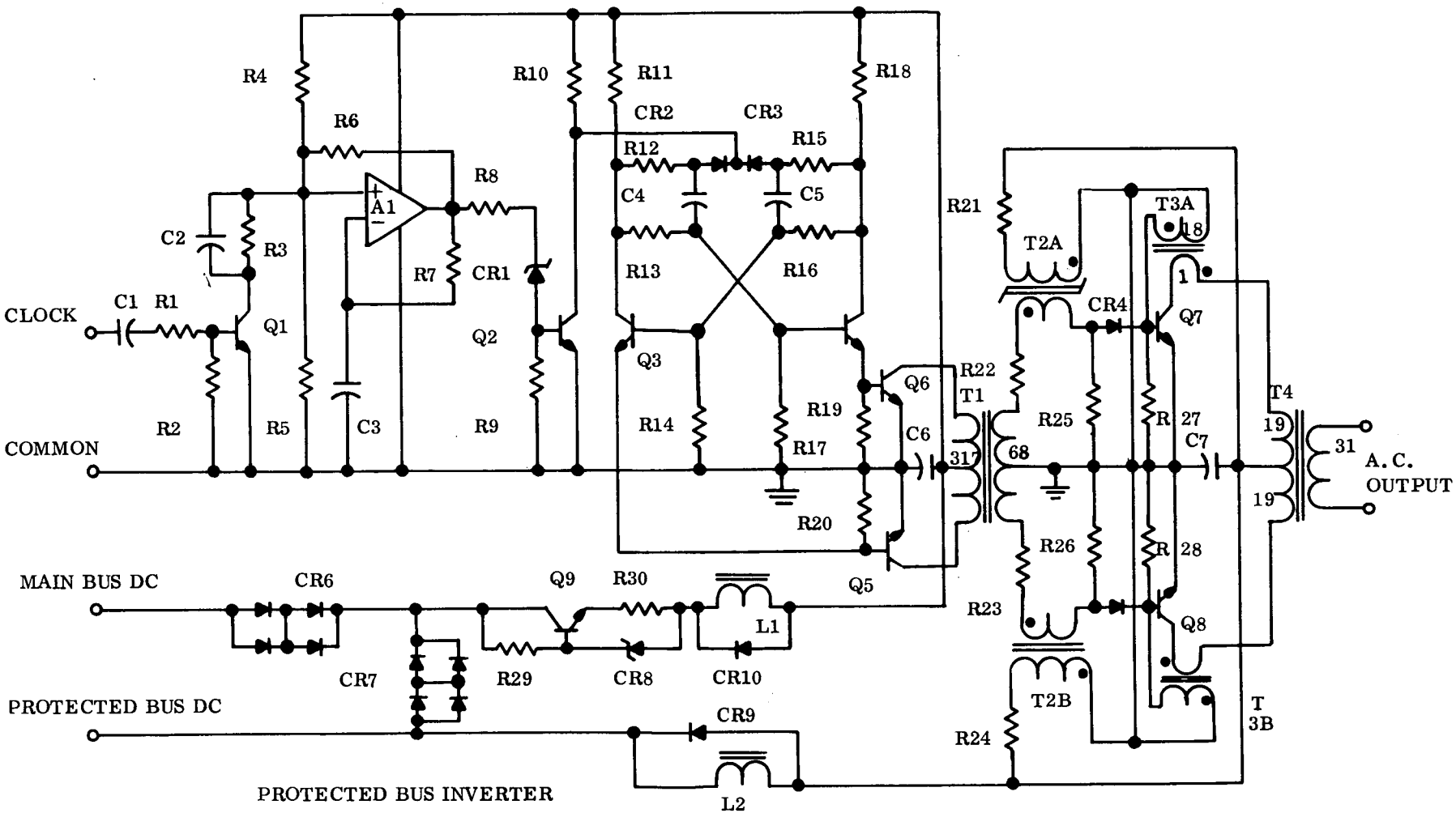


Figure 5.5-1. Protected Bus Inverter Schematic

of oscillation of 9263 Hz is obtained, within a tolerance of ± 2%. The oscillator output is a square wave; this wave drives Q2, a buffer amplifier. The oscillator can be synchronized by the clock pulse amplifier output signal.

5.5.2.3 Bistable Multivibrator and Driver Amplifier

The multivibrator triggers on the negative transition from the collector of Q2 and provides a symmetrical square wave at half the oscillator frequency to the bases of Q5 and Q6, the driver amplifier. Driver transformer T1 supplies a square wave of voltage to drive the power amplifier.

5.5.2.4 Power Amplifier

The power amplifier is composed of the drive voltage conditioning, power transistors, current feedback, and output transformer. Each of these is discussed below.

1. Drive Voltage Conditioning

   The square wave of voltage from T1 is applied to T2, which is a "volt-second device," a few turns of wire on a small saturable core. After a few microseconds, T2 saturates and permits drive voltage to be applied to the base of the corresponding power transistor. The secondary winding has a constant bias for resetting the core.

2. Power Transistors

   The power transistors are capable of fairly rapid switching of collector current, but they have considerable storage time. The drive voltage conditioning allows some time for the transistor to stop conducting before the opposite one is driven on, avoiding "overlap" of collector current. Unfortunately, this does not work well with standard SDT8801 transistors due to the fact that the storage time is quite long and temperature dependent, increasing considerably at higher temperatures. If the drive is delayed sufficiently to avoid overlap, the rise time becomes excessive at high temperature and a voltage "step" may develop at low temperature. Otherwise, current overlap will creep in at high temperature, causing efficiency to be out of specification.

3. Current Feedback

In order to obtain 11 amperes of collector current with an overloaded output, sufficient base drive must be provided. To avoid excessive overdrive under normal conditions, a current feedback transformer is used. At light loads, this circuit is relatively inactive, but as the load increases, some collector power is fed back to the base to supplement the normal drive. Thus, over 600 mA of base drive is available under overload but only on the order of 100 mA at light loads.

4. Output Transformer

The output transformer used in the breadboard operates at a flux density of approximately 5000 gauss. A new design is being considered which will operate at a reduced flux density to reduce the transient current at turn-on.

5.5.2.5 Miscellaneous Circuits

1. Diodes

Diodes CR6 and CR7 are connected to cause the circuit to draw all its power from the Protected Bus under normal conditions of operation. Under overload conditions the Protected Bus voltage falls and the Main Bus will be called upon to supply power to the driver circuits.

2. Filter Networks

Filter networks are provided to eliminate the greater part of any noise which may be generated by the inverter. These are composed of L1, L2, C6, and C7.

3. Surge Limiter

A surge limiter, made up of Q9 and associated components, prevents excessive currents from being drawn when the inverter is initially energized or if power is momentarily interrupted.

The transistors can be selected for recovery time or be replaced by higher speed types. Both have been done and the results bear out the above discussion. A very fast transistor gives a voltage step; a slow one gives low efficiency at high temperature and slow rise time. The recommended approach is to use fast transistors, reduce (or eliminate) the drive delay, and use an RC network in the collector to control rise time. Alternatively, selected SDT8801 transistors may be preferable, since the circuit works "as is" with these types. Conference

with the device vendor (Solitron) indicates a probable yield of about 20% of production. The criterion for transistor evaluation is the reverse recovery time (or storage time) of the base-emitter junction. This is used because the only path for discharge of this junction in the circuit is a 12-ohm resistor. The transistor base is driven with a 5 μs wide 200 mA pulse of low duty factor and allowed to decay through about 12 ohms. The base current will reverse to about 50 mA for a period of time. The storage time used for comparison is the time from the end of the pulse to the 50% point of reverse current (about 25 mA). A standard current probe may be used (Figure 5.5-2). Satisfactory devices are those exhibiting recovery times of 13 μs or less at any temperature (Figure 5.5-3); however, since this parameter has a positive variation with temperature, a room temperature value of 10 μs or less is necessary. For comparison, the following data were taken:

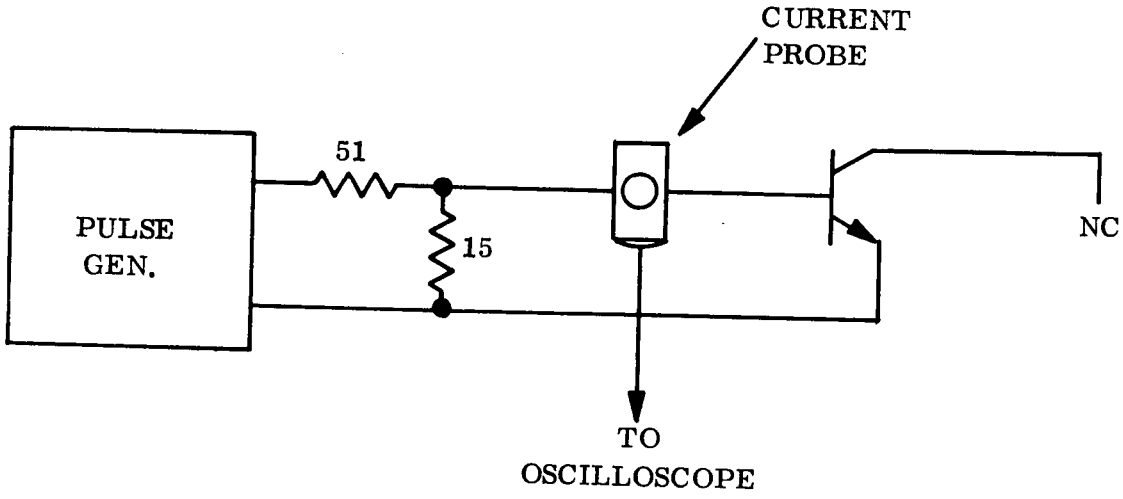


Figure 5.5-2. Transistor Test Circuit

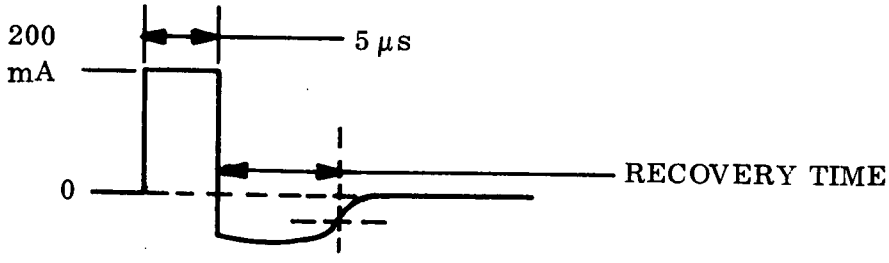


Figure 5.5-3. Recovery Time Waveform

1. Variation of recovery time with temperature of SDT8801 and 86BB114 types. Times are in μ seconds.

Temp.	SDT8801		86BB114	
	No. 1	No. 2	No. 1	No. 2
-20°C	11	9.2	6.6	7.2
25°C	14	10.5	7.7	8.5
+75°C	17	12	9.4	10

(Incidentally, the type 86BB114 works very well in the inverter but may not be used due to its epitaxial construction)

2. Variation of efficiency with recovery time.

Transistor Type	Room Temp. Recovery Time	Room Temp. Efficiency	Hi Temp. Efficiency
SDT8801	12.5 and 15 μs	94.87%	91.43%
SDT8801	13 and 7.5 μs	95.55%	93.12%
86BB114	7.7 and 8.5 μs	95.73%	95.19%
2N3265	2.5 and 4.5 μs	94.11%	94.02%
ST14032	4 and 5 μs	93.93%	94.72%

The correlation with recovery time can be seen from the above. Variations occur because other factors (such as saturation voltage) also affect the efficiency.

5.5.3 TEST RESULTS

The output voltage of the protected bus inverter was 49.375 volts minimum and 53.8 volts maximum over all variations in load, temperature and output transistors. This total variation is within the allowable voltage swing but is out of specification at the high end. This is a result of increasing the normal bus voltage from 31.75 volts to 32.2 volts. Consequently, the normal voltage will have to be adjusted downward to keep the voltage swing within the specification limits.

The rise and fall time is discussed in paragraph 5.5.2.4-2. The inverter proved to be short circuit safe for about 5 seconds at all temperatures. The frequency requirement for free running operation was met at all temperatures. The inverter's efficiency is discussed in paragraph 5.5.2.4-2. With the proper choice for power transistors, the inverter is capable of meeting the 92% minimum efficiency at all temperatures. A test of efficiency vs. input voltage showed negligible variation (0.08%). The inverter operated over the full range of temperature, including -35°C. Figures 5.5-4 through 5.5-7 show the variation in output voltage and efficiency vs. temperature for four types of output transistor. Figure 5.5-8 shows the line regulation of the inverter over the range of input voltage. Figure 5.5-9 depicts the variation in output voltage and efficiency vs. output power.

5.5.4 FAILURE MODE, EFFECT, AND CRITICALITY ANALYSIS

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.5-1. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

5.5.4.1 Overvoltage/Undervoltage

As with the Main Bus Inverter, the current limit circuitry in the Protected Bus Inverter reduces the magnitude of the overvoltage experienced by the switching circuits. However, unlike the Main Bus Inverter, the power output circuits will be subjected to the overvoltage condition. It is assumed that the output transformer T4 can support this increased voltage and not saturate.

The switching transistors Q7 and Q8 will experience a V_{ce} of 82 vdc, plus voltage transients due to switching as compared to the normal of 64 vdc (twice the input of 32 vdc) plus transients. However, they are rated at V_{ce} of 120 vdc so they do not present a problem.

During a Protected Bus undervoltage caused by an overload on the Main Bus, the current available to the Protected Bus Inverter decreases as the current increases into the Main Bus fault (see Figure 5.5-10). Calculations show that the inverter stops switching at about

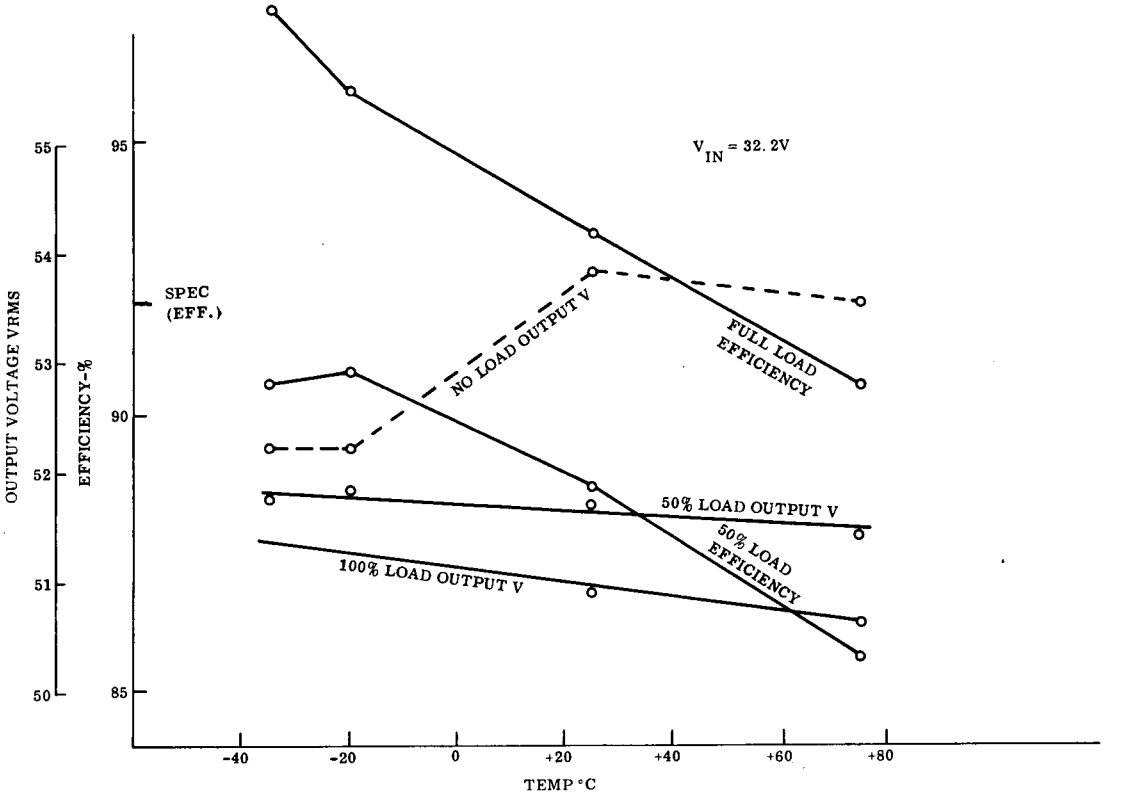


Figure 5.5-4. Protected Bus Inverter Breadboard Test Using Solitron SDT8801 (7.5 and 13.0 μs)

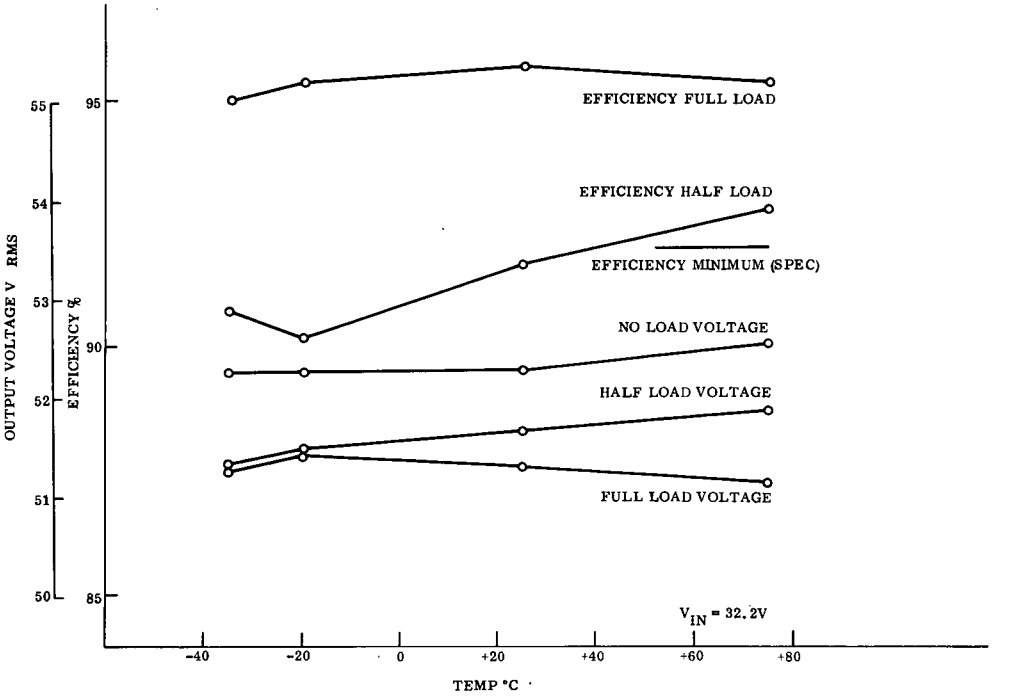


Figure 5.5-5. Protected Bus Inverter Breadboard Test Using Solitron 86BB114 (7.7 and 8.5 μs)

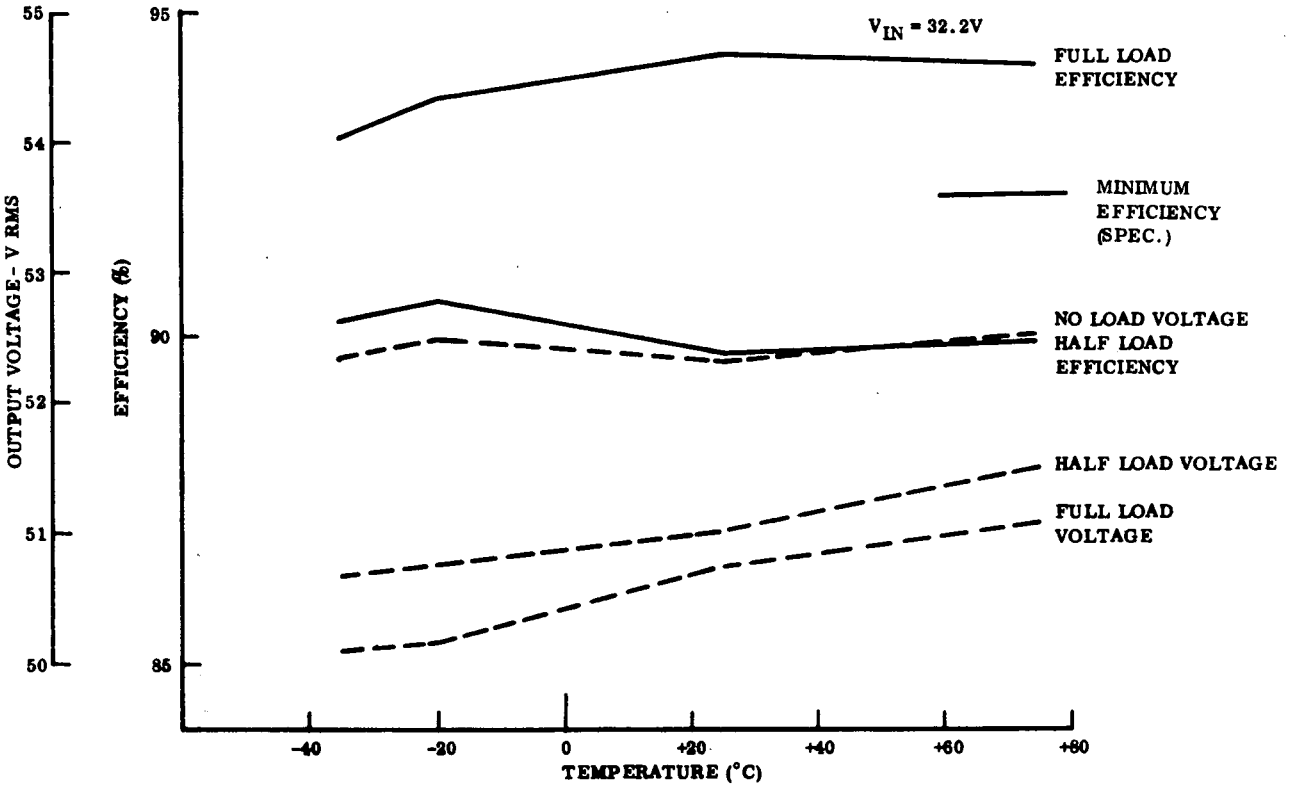


Figure 5.5-6. Protected Bus Inverter Breadboard Test Using RCA 2N3635 (2.5 and 4.5 μs)

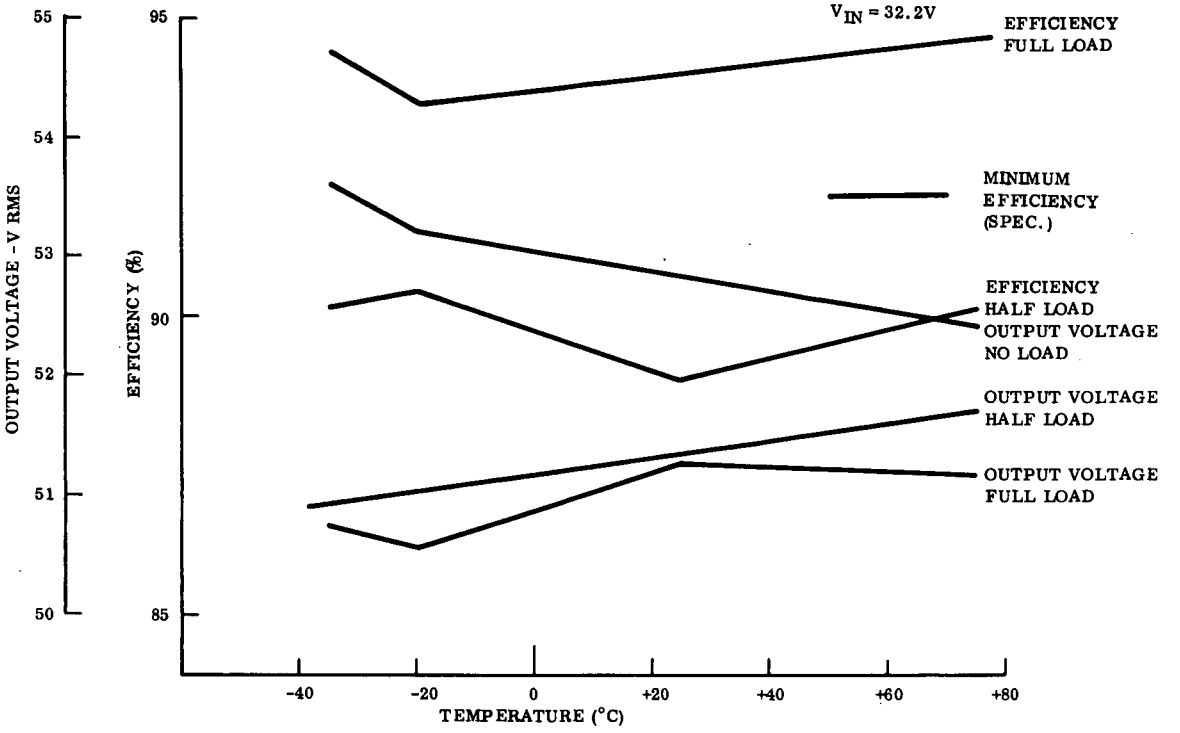


Figure 5.5-7. Protected Bus Inverter Breadboard Test Using Transitron ST14032 (4.0 and 5.0 μs)

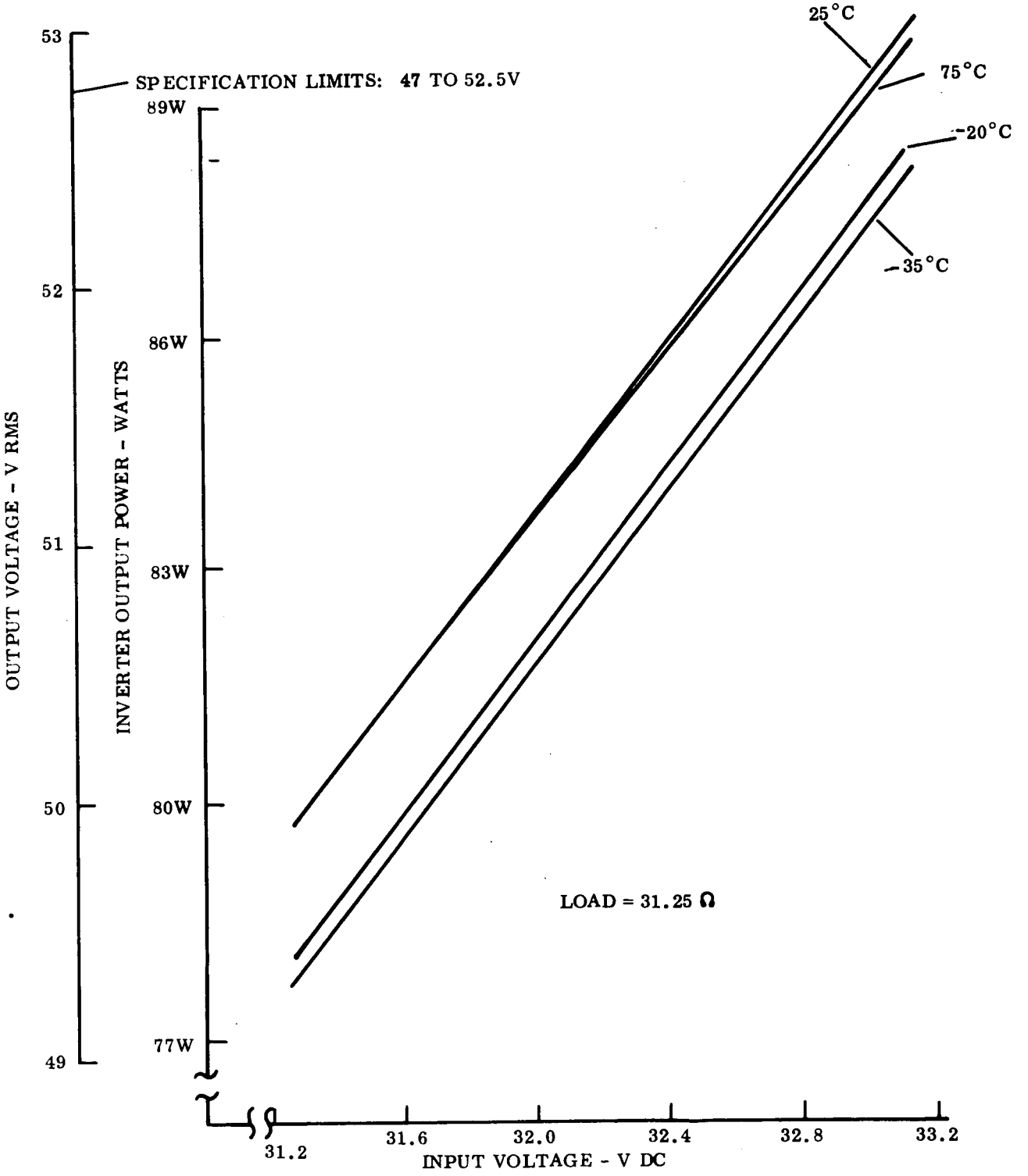


Figure 5.5-8. Output Voltage Versus Input Voltage - Line Regulation

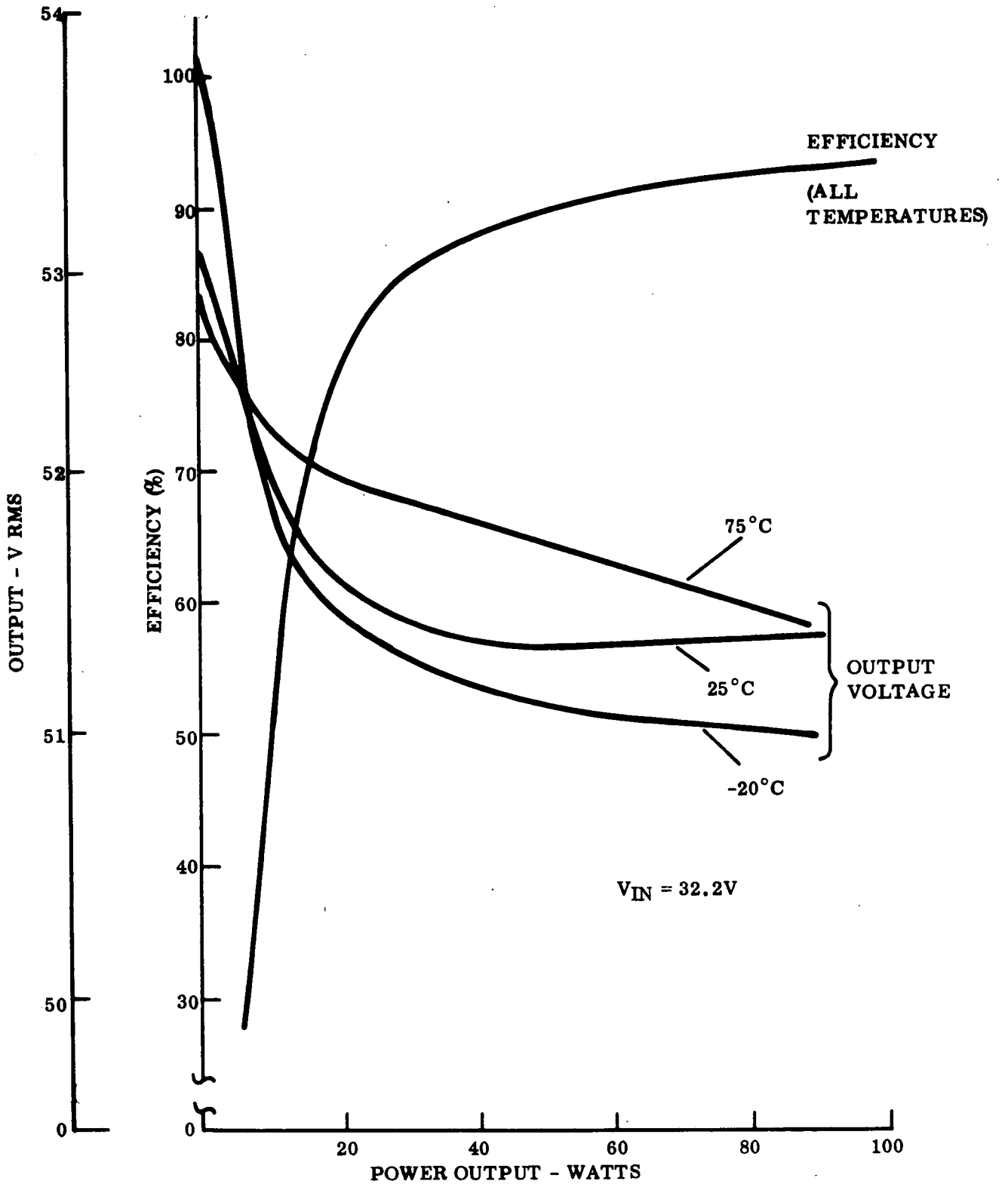


Figure 5.5-9. Protected Bus Inverter Efficiency and Output Voltage Versus Output Power (Transitron)

10 vdc. From the figure, we see that the current varies from 2 amps to 0.67 amps as the voltage drops from 30 to 10 vdc. If the output transistor does operate in its linear region, maximum power dissipation would occur when the transistor is supporting half the input voltage to the inverter. A worst case would be to assume this happens at a Protected Bus input voltage of 30 vdc at 2 amperes saturated collector current. If the transistor supported 15 vdc, only 1 ampere would flow hence the power dissipated would be 15 watts. The transistor is rated at 100 watts @ Tc = 150°C. This then, is not anticipated to be a problem.

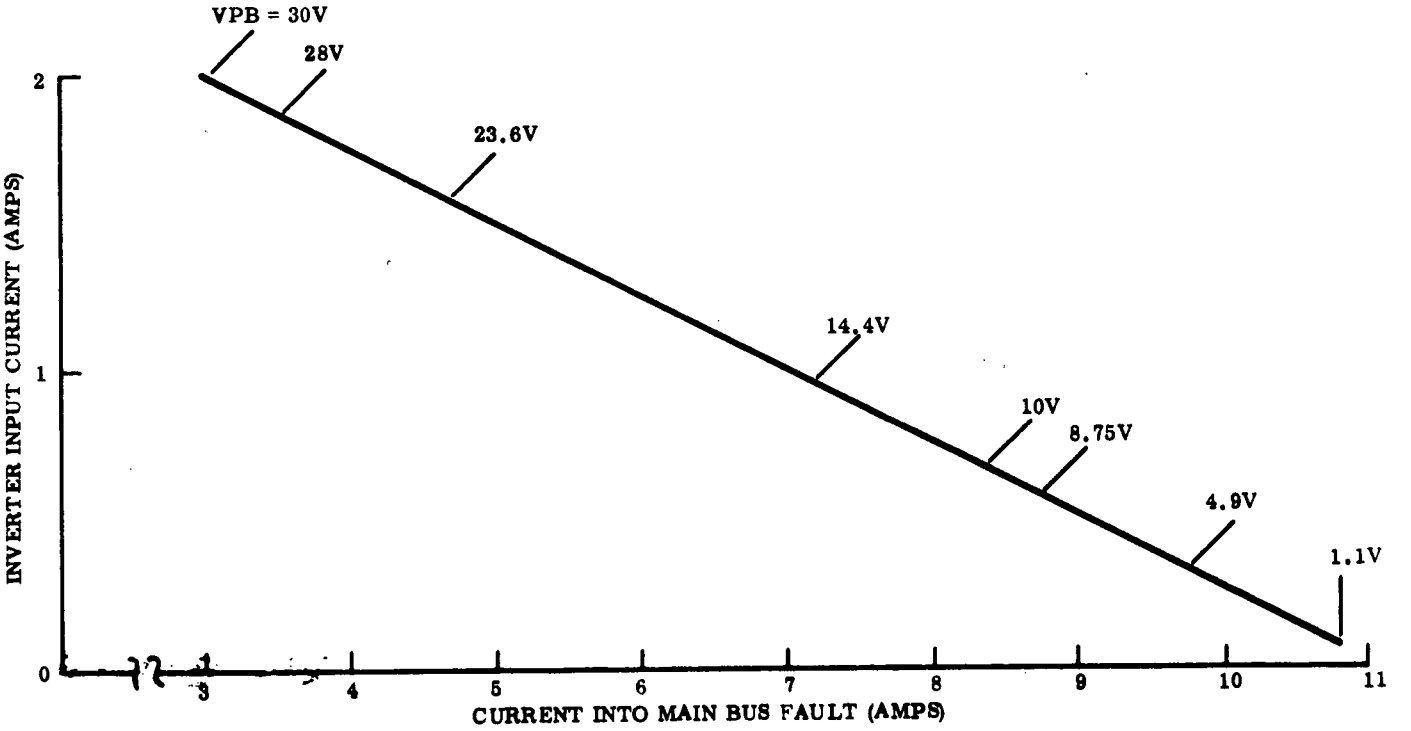


Figure 5.5-10. Protected Bus Inverter Current for Main Bus Inverter Failure

The transistors Q5 and Q6 are rated at 1 watt. The op amp oscillator circuit is the same as that used in the Main Bus Inverter, and the effects of undervoltage are the same. The op amp oscillator is likely to stop switching at 10 volts or less. When the T1 transformer saturates, the 10 volts would be dropped across the current limiter and transistors Q5 or Q6. The current limiter restricts the current to 100 milliamps. At 100 milliamps, it drops 5 of the 10 volts so the transistor Q5 or Q6 has the remaining 5 volts across it with 100 milliamps through it or a power dissipation of 500 milliwatts (half the rating of the transistor).

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	A1	Amplifier Operational	Provides switching reference for Protected Bus Inverter in Conjunction with external clock signal.	Output High		Loss of switching capability of Q2 since it will never turn off	Loss of Inverter output		
				Output Low		Loss of switching capability of Q2 since it will never turn on	Loss of Inverter output		
2	C1	Capacitor	Capacitively couple the clock pulses to the base of transistor, Q1	Open		Loss of capability of running the Inverter off the clock.	Loss of capability to synch the Inverter output		Inverter can still operate free running
				Short		None unless Q1 fails short	None		
3	C2	Capacitor	Provides a low impedance path between the non-inverting input of Op Amp-A1 and ground when Q1 turns on.	Open		Delay the response to the clock pulse	None		
				Short		Increases the power dissipation in Q1	None		
4	C3	Capacitor	Determines the free-running frequency of the oscillator in conjunction with R7	Open		Oscillation of A1 will either become uneven at a very high rate or it will hang-up in one of the two stable states	Loss of Inverter Output		
				Short		Holds the inverting input of A1 low resulting in loss of oscillation in A1, resulting in loss of switching capability of Q2.	Loss of Inverter output		

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
5	C4	Capacitor	Provides for speed-up of the switching of the transistor, Q4.	Open		Loss of switching in the multivibrator	Loss of Inverter output		
	NOTE: In conjunction with Q3, C5 has the same effects as C4			Short	failure modes and	Delays the switching response of Q4 to the A1 output	None		
6	C6	Capacitor	Provides an AC low impedance path for filtering voltage ripple on the Main Bus.	Open		Prevents filtering of the voltage ripple on the Main Bus	Could cause EMI problems with other components		
				Short		Driver transformer voltage is reduced to zero.	Loss of Inverter output		
7	C7	Capacitor	Provides an AC low impedance path for filtering voltage ripple on the Protected Bus.	Open		Prevents filtering of the voltage ripple on the Protected Bus.	Could cause EMI problems with other components		
				Short		Output transformer primary voltage is reduced to zero	Loss of Inverter output		
8	CR1	Zener Diode	Prevents Q2 from erroneously turning on when the output of A1 is low but still high enough to forward bias the base emitter of Q2.	Open		Loss of switching reference, since Q2 never turns on	Loss of Inverter output		
				Short		Loss of switching reference since Q2 never turns off	Loss of Inverter output		

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
9	CR2	Diode	Prevents charging of C4 up to the Main Bus voltage thru R10.	Open		Loss of switching in the multivibrator since Q4 cannot be turned off.	Loss of Inverter output		
				Short		Excess voltage on C4 will reverse bias the base-emitter junction of Q4 resulting in failure of Q4	Loss of Inverter output		
	NOTE: In conjunction with Q3 and C5, CR3 has the same failure modes and effects as CR2								
10	CR4	Diode	Prevents reverse bias of Q7 base to emitter when Q8 is on.	Open		Prevents forward biasing of Q7	Loss of Inverter output		
				Short		Possibility of Q7 early turn on.	Possibility of current spikes on DC bus.		
	NOTE: In conjunction with Q8, CR5 has the same failure modes and effects as CR4.								
11	CR6	Diode	Protects the Protected Bus from a short on the Main Bus	Open		Loss of Main Bus to the Driver Amplifier	None		Replace single diode with a quad redundant configuration
				Short		None unless the Main Bus fails short	None		
12	CR7	Diode	Protects the Main Bus from a short on the Protected Bus	Open		Loss of Protected Bus supply to the Driver Amplifier	None		Replace single diode with a quad redundant configuration
				Short		None unless the Protected Bus fails short	None		

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
13	CR8	Zener Diode	Determines the maximum amount of current drawn from the D.c. Bus	Open		Q9 remains full on independent of the voltage drop across R30	Current limiting in the Inverter is lost.		
				Short		Q9 turns off, inhibiting voltage to the switching circuits	Loss of Inverter output		
14	CR9	Diode	Provides a low impedance path for transient voltage spikes when the Protected Bus is turned off	Open		Develops transient voltage spikes on the bus when the Protected Bus is turned off	Could cause EMI problems with other components		
				Short		Loss of filtering of the current ripple on the Protected Bus	Could cause EMI problems with other components		
15	L1	Inductor	Provides for filtering of the current ripple on the Main Bus	Open		Loss of Protected Bus supply to the output Transformer	Loss of Inverter output		
				Short		Loss of filtering of the current ripple on the Protected Bus	Could cause EMI problems with other components		
16	L2	Inductor	Provides for filtering of the current ripple on the Protected Bus	Open		Loss of Main Bus supply to the Driver Transformer	Loss of Inverter output		
				Short		Loss of filtering of the current ripple on the Main Bus	Could cause EMI problems with other components		

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
17	Q1	Transistor	Amplifies the low level signal from the clock	Open		Loss of clock pulse reference	Loss of capability to synch the Inverter output		Inverter can still operate free running
				Short		Loss of clock pulse reference	Loss of capability to synch the Inverter output		Inverter can still operate free running
18	Q2	Transistor	Amplifies the output of the Op Amp-A1	Open		Loss of switching reference	Loss of Inverter output		
				Short		Loss of switching reference	Loss of Inverter output		
19	Q5	Transistor	In conjunction with T1, converts the 30V DC bus to a low voltage AC reference which provides the drive for the power transistor	Open		Driver transformer saturates resulting in loss of drive to the power transistors	Loss of Inverter output		
				Short		Driver transformer saturates resulting in loss of drive to the power transistors	Loss of Inverter output		
	NOTE: Q6 has the same failure modes and effects as Q5								
20	Q3	Transistor	Provides a square wave input to the base of the switching transistor in the Driver Transformer	Open		Loss of switching in the multi Vibrator	Loss of Inverter output		
				Short		Loss of switching in the multivibrator	Loss of Inverter output		
	NOTE: Q4 has the same failure modes and effects as Q3								

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
21	Q7	Transistor	Provides switching of the output transformer, T4.	Open		Output transformer saturates	Loss of Inverter output		
				Short		Output transformer saturates	Loss of Inverter output		
	NOTE: Q8 has the same failure modes and effects as Q7								
22	Q9	Transistor	Acts as the pass element in the surge limit circuitry which limits the amount of current drawn by the inverter	Open		Loss of voltage to switching circuits	Loss of Inverter output		
				Short		Q9 fails to limit the current to the switching circuits			Current limiting in the Inverter is lost.
23	R1	Resistor	Limits the base current to Q1	Open		Loss of clock reference	Loss of capability to synch the Inverter output		Inverter can still operate free running
24	R2	Resistor	Leakage resistor for Q1	Open		Q1 could turn on if leakage current was high resulting in loss of clock reference	Loss of capability to synch the Inverter output		Inverter can still operate free running
25	R3	Resistor	Discharge resistor for C2	Open		C2 cannot discharge resulting in the loss of clock reference	Loss of capability to synch the Inverter output		Inverter can still operate free running
26	R4	Resistor	In conjunction with R5 provides a voltage divider to bias the non-inverting input of A1	Open		Non-inverting input of A1 remains low causing output of A1 to remain low resulting in a loss of switching	Loss of Inverter output		

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
27	R5	Resistor	In conjunction with R4 provides a voltage divider to bias the non-inverting input of A1	Open		Non-inverting input of A1 remains high, resulting in inability to operate Inverter free-running	None unless the clock reference fails		Inverter can still operate from the clock reference
28	R6	Resistor	Feedback resistor which provides hysteresis to the non-inverting input of A1	Open		Loss of hysteresis to the non-inverting input	None unless the clock reference fails		Inverter can still operate from the clock reference
29	R7	Resistor	In conjunction with C3, determines the charge rate of C3	Open		Inverting input of A1 remains low causing the output of A1 to stay high resulting in a loss of switching	Loss of Inverter output		
30	R8	Resistor	Limits the base current to Q2	Open		Loss of drive to Q2 and loss of switching reference	Loss of Inverter output		
31	R9	Resistor	Leakage resistor for Q2	Open		Q2 could turn on if leakage current was high resulting in loss of switching reference	Loss of Inverter output		
32	R10	Resistor	Limits the collector current of Q2	Open		Might reduce the rise/fall time of multivibrator.	NONE		
33	R11	Resistor	Limits the collector current of Q3			Loss of ability to turn on Q4 resulting in loss of switching in the multivibration	Loss of Inverter output		
	NOTE: In conjunction with Q4, R18 has the same failure modes and effects as R11.								

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
34	R12	Resistor	Controls the charge time of C4			Loss of ability to charge C4 resulting in delay at response of Q4 to output of A1	Loss of Inverter output.		
NOTE:	In conjunction with C5, R15 has the same failure modes and effects as R12.								
35	R13	Resistor	Limits the current to the base of Q4 after C4 is fully charged			Loss of ability to turn on Q4 resulting in loss of switching in the multivibrator	Loss of Inverter output		
NOTE:	In conjunction with Q3 and C5, R16 has the same failure modes and effects as R13								
36	R14	Resistor	Leakage resistor for Q3			Q3 could turn on if leakage current was high resulting in loss of switching reference	Loss of Inverter output		
NOTE:	In conjunction with Q4, R17 has the same failure modes and effects as R14.								
37	R19	Resistor	Leakage resistor for Q6			Q6 could turn on if leakage current was high resulting in loss of switching reference	Loss of Inverter output		
NOTE:	In conjunction with Q5, R20 has the same failure modes and effects as R19.								
38	R21	Resistor	Limits the current in the reset winding of the volt-second device, T2			Loss of capability to reset T2A, resulting in loss of delay of Q7 turn-on.	Large current spikes on the DC Bus caused by shoot-through current.		
NOTE:	In conjunction with Q7 and T2B, R24 has the same failure modes and effects as $21.								
39	R22	Resistor	Limits the current to the base of the power transistor, Q7			Loss of base drive to Q7, causing primary of T4 to saturate	Loss of Inverter output		
NOTE:	In conjunction with Q8, R23 has the same failure modes and effects as R22.								

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
40	R25 NOTE: In conjunction with Q8, R26 has the same failure modes and effects as R25.	Resistor	Provides a path for the magnetizing current while the volt-second device is supporting voltage			T2 magnetization current could turn Q7 on prematurely	Large current spikes on the DC Bus caused by short-through current		
41	R27 NOTE: In conjunction with Q8, R28 has the same failure modes and effects as R27.	Resistor	Leakage resistor for Q7			Q7 could turn on if leakage current was high causing primary of T4 to saturate	Loss of Inverter output		
42	R29	Resistor	Provides the base current for Q9, and the sensor current for CR8			Q9 turns off resulting in loss of voltage to switching circuits	Loss of Inverter output		
43	R30	Resistor	Determines the magnitude of the current limit	Open		Loss of voltage to switching circuits	Loss of Inverter output		
44	T1	Transformer, Driver	Supplies a square wave of voltage to drive the power amplifier	Open Winding		Loss of drive to one or both of the power transistors	Loss of Inverter output		
				Shorted Winding		Overload current might cause a failure in Q5 or Q6 when the transformer saturated	Loss of Inverter output		

Table 5.5-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem Power
Component Protected Bus Inverter
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
45	T2	Volt-Second Device	Controls the application of drive voltage to the base of the power transistors Q7 and Q8	Open Winding in Primary		Loss of base drive to power transistors and loss of T2 function	Loss of Inverter output		
				Open Winding in Secondary		Loss of delay provided by volt-second device.	Possibility of overlap in transistor switching		
				Shorted Winding		Loss of delay provided by volt-second device	Possibility of overlap in transistor switching		
46	T3	Transformer, Current	Controls the application of base drive to the power transistors as a function of the load demand.	Open Winding in Primary		Loss of switching by power transistors	Loss of Inverter output		
				Open Winding in secondary		Loss of increased base drive to power transistors.	Insufficient base drive under heavy load		
				Shorted Winding in Primary		Loss of increased base drive to power transistors.	Insufficient base drive under heavy load		
				Shorted Winding in Secondary		Base to emitter short on power transistor.	Loss of Inverter output		
47	T4	Transformer, Output	Supplies the output voltage of the inverter	Open Winding		Loss of Inverter output	Loss of Inverter output		
				Shorted Winding		Overload current would probably cause a failure in Q7 or Q8 when the transformer saturated	Loss of Inverter output		

5.6 INVERTER SWITCH

5.6.1 FUNCTIONAL REQUIREMENTS

The power distribution assembly of the power conditioning equipment (PCE) contains four switches for the inverter functions: Main Bus Inverter Input, Main Bus Inverter Output, Protected Bus Inverter Input, and Protected Bus Inverter Output. The overriding requirement on the four inverter switches is that no single failure shall cause or prevent change of state of the switch. Both the input and output switches for the main bus inverter are to be capable of operation once, following the loss of both buses. The input and output switches of the protected bus inverter are to continue operation with the loss of either the main or the protected bus. To provide for operation in spite of any single failure, all four switches shall incorporate redundant operation in both the make and break functions in order to provide for resetable turn-on and turn-off. Both input switches shall perform dc switching while both output switches perform ac switching. The maximum currents for the make and break functions of the four switches are listed below:

Table 5.6-1. Inverter Switches Make and Break Currents

Inverter Switch	Make Current	Break Current
Main-Input	10.0A	34.0A
Main-Output	5.5A	20.5A
Protected-Input	2.5A	11.0A
Protected-Output	1.5A	6.6A

5.6.2 DESIGN DESCRIPTION (FIGURE 5.6-1)

The Inverter Switch is designed to provide load turn-on and turn-off capability on command from either of two signal sources. The capability to operate once after the loss of both buses is accomplished by providing energy storage in the form of a charged capacitor. To provide for redundant make and break functions, the switch is, of course, configured in a quad. Each quarter of the quad is provided with its own relay coil supply line and correspondingly its own energy storage capacitor. The switch will operate from the 30.0 ± 0.3 volt main bus or the

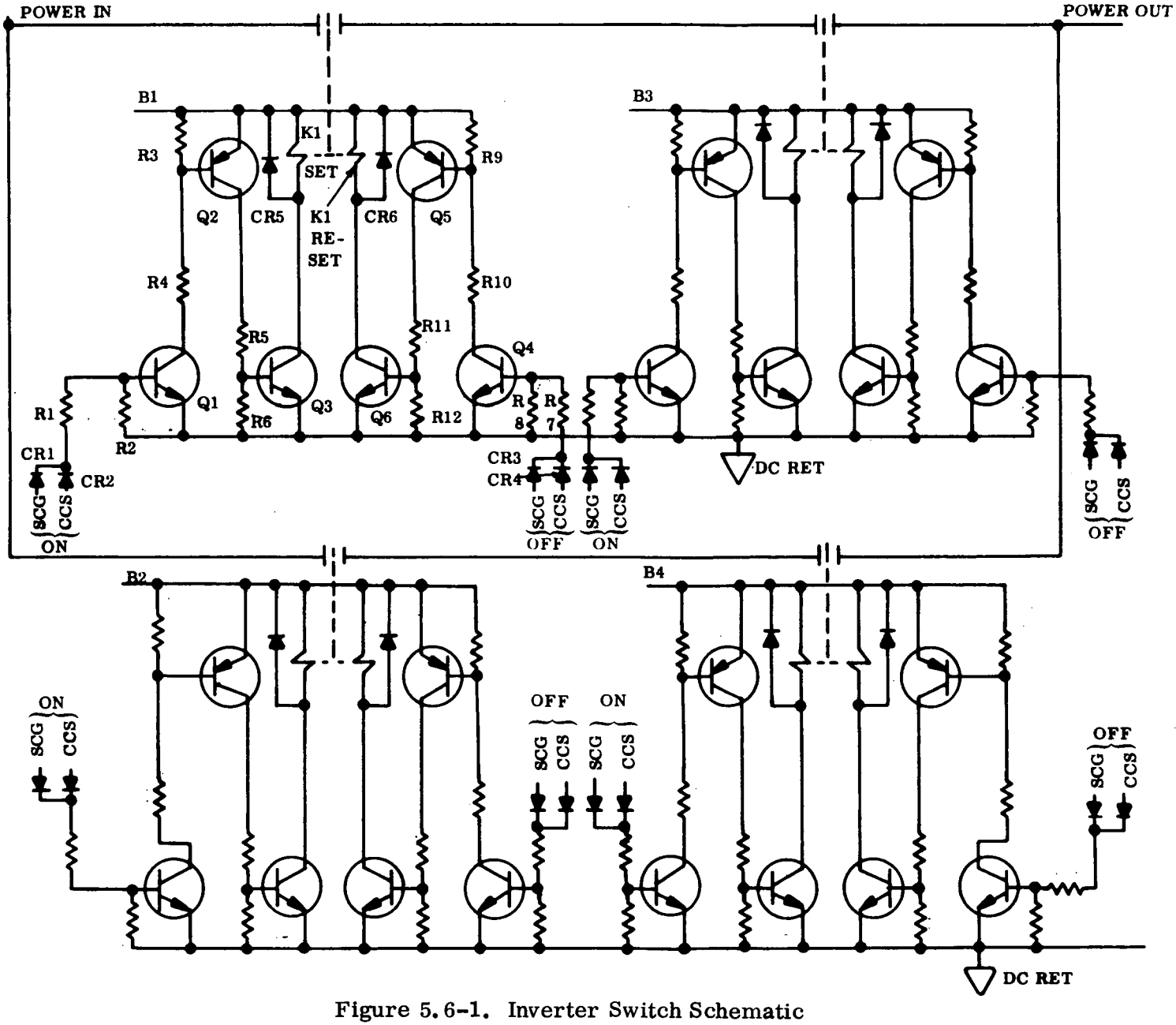


Figure 5.6-1. Inverter Switch Schematic

32.2 $\pm$ 0.9 volt protected bus, and be capable of switching 50 volts ac. The detailed circuit design is such that no single piece part failure shall prevent subsequent turn-on or turn-off of the switch.

5.6.3 TEST RESULTS

No breadboard tests of the inverter switch were performed. The theory of operation of the switch was verified in the testing of the power distribution switch, since schedules did not permit a separate test of both switches.

5.6.4 FAILURE MODE, EFFECT, AND CRITICALITY ANALYSIS

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.6-2. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

Table 5.6-2. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component INVERTER QUAD SWITCH
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	CR1	Diode	Provides isolation from the command source in the event it fails low. (short to ground)	Open		SW #1 will not respond to the On command from Cmd source #1		SW #1 can be operated from Cmd source #2	
				Short		NONE	None unless a command source has a failure low. Then none of the four switches in the quad could be commanded to the On state.		
NOTE:	Diode CR 2 has the same failure modes and effects as CR1 above except it protects from failures of the second command source.								
2	CR3	Diode	Provides isolation from the command source in the event it fails low.(short to ground)	Open		SW #1 will not respond to the Off command from Cmd source #1		SW #1 can be operated from Cmd source #2	
				Short		NONE	None unless a command source has a failure low. Then none of the four switches in quad could be commanded to the Off state.		
NOTE:	Diode CR 4 has the same failure modes and effects as CR 3 above except it protects from failure of the second command source.								

Table 5.6-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component INVERTER QUAD SWITCH
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
3	CR5	Diode	Relay coil transient suppression	Open		Current spike on DC line when Q3 shuts off	Could cause interference with other circuits.		
				Short		K1 set coil could not be energized. Can't close SW #1.	Will produce a high current drain on the DC bus when Q3 is commanded on.		Add another series diode.
4	CR6	Diode	Relay coil transient suppression	Open		Current spike on DC line when Q6 shuts off	Could cause interference with other circuits.		
				Short		K1 reset coil could not be energized. Can't open SW #1.	Will produce a high current drain on the DC bus when Q6 is commanded on.		Add another series diode.
5	R1	Resistor	Current limit base drive of Q1	Open		Can't close SW #1	NONE	SW #2, 3 & 4 can still control the quad switch state.	
6	R2	Resistor	Q1 leakage resistor	Open		Q1 could turn on if leakage current was high. This will activate the relay and close SW#1.		SW #2, 3 & 4 can still control the quad switch state.	
7	R3	Resistor	Q2 leakage resistor	Open		Q2 could turn on if leakage current was high. This will activate the relay and close SW #1.		SW #2, 3 & 4 can still control the quad switch state.	
8	R4	Resistor	Limits the current to base of Q2	Open		Base drive is lost. SW #1 can't be closed.		SW #2, 3 & 4 can still control the quad switch state.	
9	R5	Resistor	Limits the current to base of Q3	Open		Base drive is lost. SW #1 can't be closed.		SW #2, 3 & 4 can still control the quad switch state.	

Table 5.6-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component INVERTER QUAD SWITCH
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
10	R6	Resistor	Q3 leakage resistor	Open		Q3 could turn on if leakage current was high. This will activate the relay and close SW #1.		SW #2, 3 & 4 can still control the quad switch state.	
11	R7	Resistor	Limits the current to base of Q4	Open		Can't open SW #1.		SW #2, 3 & 4 can still control the quad switch state.	
12	R8	Resistor	Q4 leakage resistor	Open		Q4 could turn on if leakage current was high. This will activate the relay and open SW #1.		SW #2, 3 & 4 can still control the quad switch state.	
13	R9	Resistor	Q5 leakage resistor	Open		Q5 could turn on if leakage current was high. This will activate the relay and open SW #1.		SW #2, 3 & 4 can still control the quad switch state.	
14	R10	Resistor	Limits the current to base of Q5	Open		Base drive is lost. SW #1 can't be opened.		SW #2, 3 & 4 can still control the quad switch state.	
15	R11	Resistor	Limits the current to base of Q6	Open		Base drive is lost. SW #1 can't be opened.		SW #2, 3 & 4 can still control the quad switch state.	
16	R12	Resistor	Q6 leakage resistor	Open		Q6 could turn on if leakage current was high. This will activate the relay and open SW #1,		SW #2, 3 & 4 can still control the quad switch state.	

Table 5.6-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component INVERTER QUAD SWITCH
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
17	Q1	Transistor	Amplifies the input command signal to close SW #1	Open		SW #1 can't be closed.		SW #2, 3 & 4 can still control the quad switch state.	
				Short		K1 set coil will be energized continuously. SW #1 will remain closed.			
18	Q2	Transistor	Amplifies Q1 signal	Open		SW #1 can't be closed.		SW #2, 3 & 4 can still control the quad switch state.	
				Short		K1 set coil will be energized continuously. SW #1 will remain closed.			
19	Q3	Transistor	Amplifies Q2 signal to activate relay set coil	Open		SW #1 can't be closed.		SW #2, 3 & 4 can still control the quad switch state.	
				Short		K1 set coil will be energized continuously. SW #1 will remain closed.			
20	Q4	Transistor	Amplifies the input command signal to open SW #1	Open		SW #1 can't be opened		SW #2, 3 & 4 can still control the quad switch state.	
				Short		K1 reset coil will energized continuously. SW #1 will remain open.			

Table 5.6-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component INVERTER QUAD SWITCH
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
21	Q5	Transistor	Amplifies Q4 signal	Open		SW #1 can't be opened.		SW #2, 3 & 4 can still control the quad switch state.	
				Short		K1 reset coil will be energized continuously SW #1 will remain open			
22	Q6	Transistor	Amplifies Q5 signal to activate relay reset coil.	Open		SW #1 can't be opened		SW #2, 3 & 4 can still control the quad switch state.	
				Short		K1 reset coil will be energized continuously SW #1 will remain open			
23	K1	Mag-Latch Relay	In conjunction with 3 other relays; it opens and closes the power path to or from the inverter	Fails to close		SW #1 can't be closed		SW #2, 3 & 4 can still control the quad switch state.	
				Fails to open		SW #1 can't be opened			
24	CR7	Diode	Prevents discharger of energy storage capacitor C1 into an undervoltage protected bus	Open		C1 can't be charged from the protected bus.		C1 can be charged from the main bus via CR8.	All diodes joining the Main and Protected Buses should be quaded
				Short		Loss of isolation from PB undervoltage could prevent SW #1 of all inverter quad switches from operating during the undervoltage period.	An undervoltage on the Protected Bus will pull down the Main Bus thru CR8.	SW #2, 3 & 4 of all the quad switches are still operable.	

Table 5.6-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component INVERTER QUAD SWITCH
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
25	CR8	Diode	Prevents discharge of energy storage capacitor C1 into an undervoltage main bus.	Open		C1 can't be charged from the main bus		C1 can be charged from the protected bus via CR7	All diodes joining the Main and Protected Buses should be quaded.
				Short		Loss of isolation from MB undervoltage. Could prevent SW #1 of all inverter quad switches from operating during the undervoltage period.	An undervoltage on the Main Bus will pull down the Protected Bus thru CR 7.	SW #2, 3 & 4 of the the quad switches are still operable.	
	NOTE: Diodes CR9 thru CR14 have the same failure modes and effects as CR 7 and CR 8 above.								
26	C1	Capacitor	Provide energy to operate SW #1 of all inverter quad switches in the event that the main and protected bus voltages are low	Open		SW #1 of all inverter switches will not operate if main and protected bus voltage is low.		SW #2, 3 & 4 of all the quad switches are still operable.	
				Short		SW #1 of all inverter switches will not operate if main and protected bus voltage is low.		SW #2, 3 & 4 of all the quad switches are still operable.	Power lost due to a short will be limitec limited by R13.
	NOTE: Capacitor C2, C3 and C4 have the same failure modes and effects as C1 above except C2 operates SW #2, C3 operates SW #3, and C4 operates SW #4 in all quad switches.								
27	R13	Resistor	Limits the charge rate of capacitor C1 and limits the current drain on the main & protected buses in the event of a capacitor short circuit.	Open		C1 can't be charged. SW #1 of all inverter switches will not operate if main and protected bus voltage is low.		SW #2, 3 & 4 of all the quad switches are still operable.	
	NOTE: Resistors R14 thru R16 have the same failure modes and effects as R13 above except they effect SW#2, 3 and 4 respectively.								

5.7 INVERTER SWITCH COMMAND GENERATOR

5.7.1 FUNCTIONAL REQUIREMENTS

The inverter switch command generator provides the interface between the inverter failure detector and the inverter switches. Each module of the command generator shall operate only when its corresponding inverter is powered. Each module controls the operation of the "next" inverter. Each module shall also power the "next" module if the inverter failure detector signal is not cleared, thus choosing the third inverter if the "next" inverter fails to operate. Thus the command generator performs the logic function of deciding which inverter to turn off and which to turn on.

5.7.2 DESIGN DESCRIPTION (Figure 5.7-1)

The powering of each module by the "previous" module is performed by the seriesed transistors leading to Output No. 4 of each module. The zener, capacitor, and resistor arrangement in the base drive provides about 20 milliseconds delay before the "next" in inverter turns on. This provides immunity from system transients, but mainly it allows the inverter which has just been turned on sufficient time to prevent its command module from initiating a command to go to the next inverter. In addition, this delay also provides reset time for the failure detector.

5.7.3 TEST RESULTS

The breadboard testing of the command generator demonstrated operation within specification of all modules. The energy storage, with only 75% capacity, proved to be adequate to produce complete outputs from all three modules. The command pulses, monitored at the 62 K-ohm resistors, exceeded 10 milliseconds at ambient temperature. Temperature testing and integration with the failure detector and inverter switches should be performed at the next level in order to fully verify the design.

5.7.4 FAILURE MODE, EFFECT, AND CRITICALITY ANALYSIS

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.7-1. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

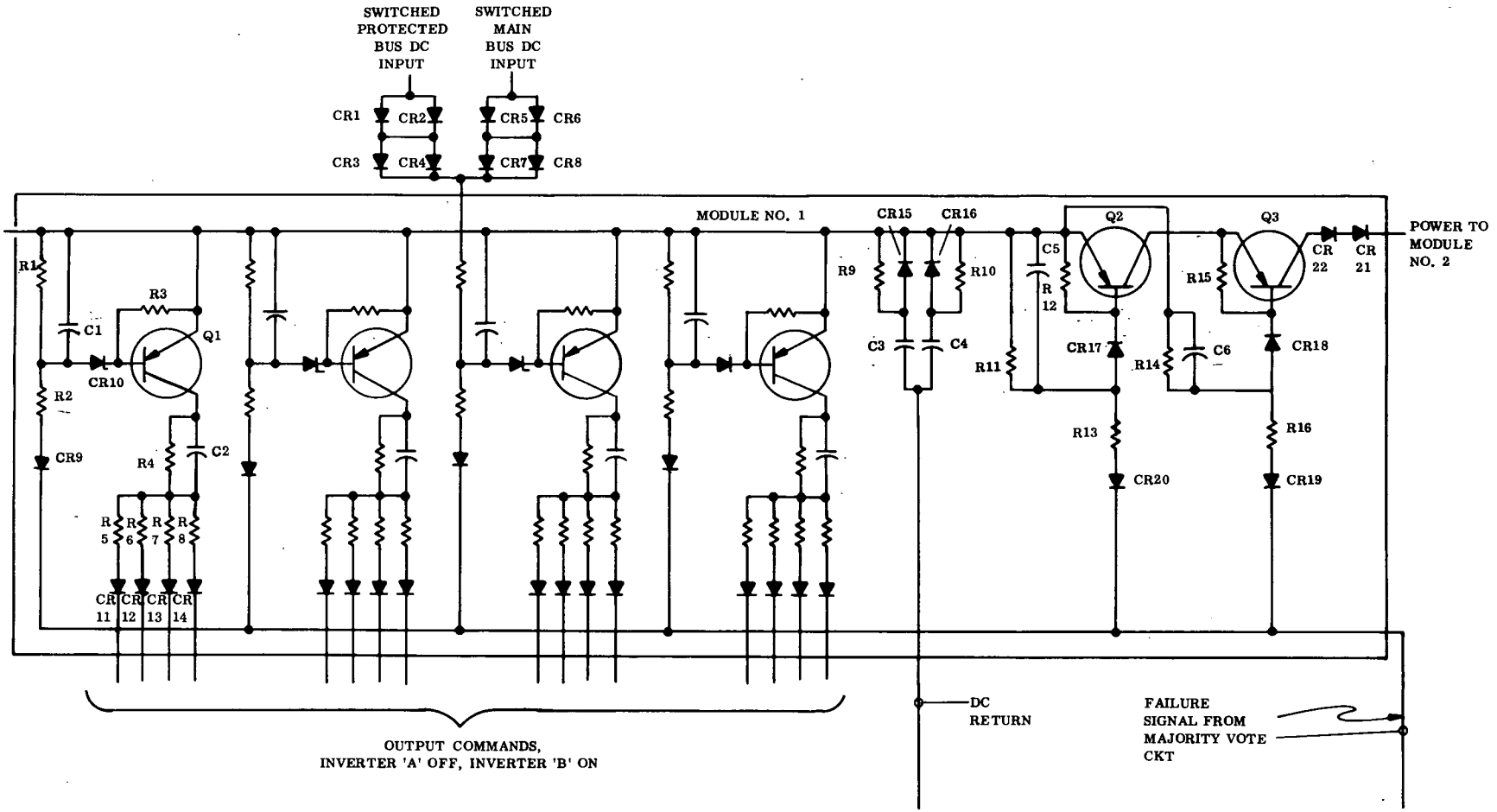


Figure 5.7-1. Inverter Switch Command Generator Schematic

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	R1	Resistor	Discharge path for time delay capacitor C1.	Open		C1 couldn't be discharged after testing the circuit.			Time delay could be lost, but only one switch in the quad would be transferred which isn't enough to change the state of the quad switch.
2	R2	Resistor	Limits the base current of Q1.	Open		Q1 won't operate when failure signal is present			
3	R3	Resistor	Q1 leakage resistor	Open		Q1 could turn on if leakage current was high.			
4	R4	Resistor	Discharge resistor for C2 A.C. coupling capacitor.	Open		Capacitor would not discharge after being charged.			
5	R5	Resistor	Limits switch command output current to the quad switch.	Open		One switch in one quad inverter switch won't respond to the Q1 command.			
	NOTE:	Resistors R6 thru R8 have the same failure modes and effects as R5 above.							
6	R9	Resistor	Limits the charge current of energy storage capacitor C3.	Open		C3 won't charge.		C3 is backed up by C4.	

Table 5.7-1. Failure Mode, Effect, and Criticality Anlysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
7	R10	Resistor	Limits the charge current of energy storage capacitor C3.	Open		C4 won't charge		C4 is backed up by C3.	
8	R11	Resistor	Provides discharge path for time delay capacitor C5.	Open		Q2 turns on as soon as the failure signal is present.		Q3 must also turn on before power from the energy storage capacitors is made available to Inverter Switch Command #2.	
9	R12	Resistor	Q2 leakage resistor	Open		Q2 could turn on if leakage current was high.		Q3 must also turn on before power from the energy storage capacitors is made available to Inverter Switch Command #2.	
10	R13	Resistor	Limits base current of Q2	Open		Q2 won't turn on when failure signal is present.	If both Main and Protected Buses are low and the inverter being switched on is failed, the #2 ISCG can't turn on the third inverter.		

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
11	R14	Resistor	Provides discharge path for time delay capacitor C6.	Open		Q3 turns on as soon as the failure signal is present.		Q2 must also turn on before power from the energy storage capacitors is made available to Inverter Switch Command Generator #2.	
12	R15	Resistor	Q3 leakage resistor	Open		Q3 could turn on if leakage current was high.		Q2 must also turn on before power from the energy storage capacitors is made available to Inverter Switch Command Generator #2.	
13	R16	Resistor	Limits base current of Q3.	Open		Q3 won't turn on when failure signal is present.	If both Main and Protected Buses are low and the inverter being switched on is failed, the #2 ISCG can't turn on the third inverter		
14	CR1	Diode	Provides isolation of other power sources from an undervoltage on the Procteeted Bus.	Open or Short		NONE		Diode is part of a quad. Operation is not effected by any signal failure.	
	NOTE:	CR2 thru CR4 are part of the diode quad of CR1.							

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
15	CR5	Diode	Provides isolation of other power sources from an under-voltage on the Main Bus	Open or Short		NONE		Diode is part of a quad. Operation is not effected by any signal failure.	
	NOTE:	CR6 thru CR8 are part of the diode quad of CR5.							
16	CR9	Diode	Majority vote ckt. signal is common to both #1 & #2 cmd. generator modules. This signal is high when there is no failure. Without CR9, the energy storage capacitors of #2 modules would charge up thru the R1-R2 sneak path. When the failure signal goes low, both #1 & #2 cmd. generator modules would provide switch commands. #1 cmd. generator tries to turn	Open		Q1 won't turn on when failure signal is present.			Only one switch in each quad switch fails to work. The three switches remaining still have control.

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
16			off inverter #1 and turn on inverter #2 while #2 cmd. generator tries to turn off inverter #2 and turn on inverter #3.						
				Short		See Function	See Function		
17	CR10	Zener Diode	In conjunction with C1, provides a time delay for Q1 turn on.	Open		Q1 won't turn on when failure signal is present.			
				Short		Q1 turn on delay is lost.		Q1 operates only one switch in a quad switch. Other switches will still be delayed.	
18	CR11	Diode	Provides isolation at the inverter switch command interface in the event of a short to ground in the command generator.	Open		One switch in an inverter quad switch will not respond to the command from Q1.			

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
18				Short		None - unless there is a short to ground in the Command Generator.			
	NOTE: Diodes CR12 thru CR14 have the same failure modes and effects as CR11 above.								
19	CR15	Diode	Provides discharge path for energy storage capacitor C3.	Open		Discharge time constant thru R9 would be too long to provide power to the Command Generator		This energy storage circuit is backed-up by redundant C4 circuit.	
				Short		Capacitor charge current would be limited by only the RTG impedance and the inverter choke.			
	NOTE: Diode CR16 performs the same function as CR15 except for capacitor C4.								
20	CR17	Zener Diode	In conjunction with C5, provides a time delay for Q2 turn on.	Open		Q2 won't turn on when failure signal is present.			Power from energy storage circuits would not be available to the second command generator. If both the PG & MB were low, and the #2 inverter that was just switched on was bad, there would be no way that the second cmd.

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
20									generator could turn on #3 inverter.
				Short		Q2 turn on delay in lost		Q3 which is also delayed, must turn on before power is applied to the second command generator.	
	NOTE:	Zener Diode CR18 performs the same function as CR17, except CR17, except for transistor Q3.							
21	CR19	Diode	Provides the same function as diode CR9 except for a different combination of sneak path resistors.	Open		Q3 won't turn on when failure signal is present.			Power from energy storage circuits would not be available to the second command generator. If both the PG & MB were low, and the #2 inverter that was just switched on was bad, there would be no way that the second cmd. generator could turn on #3 inverter.
				Short		See Function of CR9	See Function of CR9		

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
22	CR20	Diode	Provides the same function as diode CR19 and CR9 except for a different combination of sneak path resistors.	Open		Q2 won't turn on when failure signal is present.			Power from energy storage circuits would not be available to the second command generator. If both the PG & MB were low, and the #2 inverter that was just switched on was bad, there would be no way that the cmd. generator could turn on #3 inverter.
				Short		See Function of CR9	See Function of CR9		
23	CR21	Diode	Prevents voltage of #2 cmd. generator from charging capacitors in #1 cmd. generator after #1 has been used.	Open		No output power to #2 cmd. generator from the energy storage capacitors.			Power from energy storage circuits would not be available to the second command generator. If both the PG & MB were low, and the #2 inverter that was just switched on was bad, there would be no way

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
									that the cmd. generator could turn on #3 inverter.
				Short		NONE		CR21 is backed-up by series redundant CR22.	
24	CR22	Diode	Prevents voltage of #2 cmd. generator from charging capacitors in #1 cmd. generator after #1 has been used.	Open		No output power to #2 cmd. generator from the energy storage capacitors.			Power from energy storage circuits would not be available to the second command generator. If both PG & MB were low, and the #2 inverter that was just switched on was bad, there would be no way that the cmd. generator could turn on #3 inverter.
				Short		NONE		CR22 is backed-up by series redundant CR21.	

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
25	C1	Capacitor	Delay turn on of Q1	Open		Loss of delay. Q1 turns on when failure signal is present.		Delay in switching inverters is still provided as other three switches in the quad switch are delayed.	
				Short		Q1 won't turn on.		One switch in each inverter quad switch won't operate. The three other switches in the quad are sufficient.	
26	C2	Capacitor	A.C. couple the switch commands so that a failure short of Q1 won't keep the command outputs high.	Open		Loss of commands of Q1		One switch in each inverter quad switch won't operate. The three other switches in the quad are sufficient.	
				Short		No effect unless Q1 fails short.			
27	C3	Capacitor	Provide energy storage in the event that both PB & MB voltage are low.	Open or Short		NONE		C3 is backed-up by C4. Only one is required.	

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
28	C4	Capacitor	Provide energy storage in the event that both PB & MB voltage are low.	Open or Short		NONE		C4 is backed-up by C3. Only one is required.	
29	C5	Capacitor	Delays turn on of Q2. Q2 is to be turned on only if the inverter failure persists for a long time.	Open		Q2 turns on when failure signal is present. Loss of delay.		Q3 must also turn on and it still has its delay.	
				Short		Q2 won't turn on.			
	NOTE:	Capacitor C6 performs the same function as C5 except for transistor Q3.							
30	Q1	Transistor	Provides commands to one switch in each of four inverter quad switches to turn off a failed inverter and turn on the standby inverter.	Open		The commands to the switches are not generated.		One switch in each inverter quad switch won't operate. The three other switches in the quad are sufficient.	
				Short		The commands are prematurely sent to the switches.		One switch in each quad changes state but this isn't enough to change the quad state.	

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
31	Q2	Transistor	Provides power to the #2 cmd. generator from the #1 cmd. generator energy storage capacitors in the event that PB & MB voltages are low, and the second inverter that was switched on was bad and the third inverter must be turned on.	Open		Power transfer to the #2 cmd. generator can't be accomplished.			It takes many failures before this has an effect. Must have 2 failures to loose PB voltage. First inverter must fail and then the second inverter that was turned on had failed during its dormancy period such that it pulls down the MB when switched on. Now if this transistor has failed open, it is the fifth failure in the Power S/S.
				Short		NONE		Q2 is backed-up with series redundant Q3.	

Table 5.7-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER SWITCH COMMAND GENERATOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
32	Q3	Transistor	Provides power to the #2 cmd. generator from the #1 cmd. generator energy storage capacitors in the event that PB & MB voltages are low, and the second inverter that was switched on was bad and the third inverter must be turned on.	Open		Power transfer to the #2 cmd. generator can't be accomplished.			It takes many failures before this has an effect. Must have 2 failures to loose PB voltage. First inverter must fail and then the second inverter that was turned on had failed during its dormancy period such that it pulls down the MB when switched on. Now if this transistor has failed open, it is the fifth failure in the Power S/S.
				Short		NONE		Q3 is backed-up with series redundant Q2.	

5.8 INVERTER FAILURE DETECTOR

5.8.1 FUNCTIONAL REQUIREMENTS

The failure detector determines if an inverter has failed. It must distinguish a true inverter failure from all other type failures which can cause either excess currents or bus undervoltages. The inverter failure detector must have a high order of reliability and be immune to those single failure modes which would cause large system perturbations. The detection/switching arrangement must be capable of detecting and switching out a failed inverter and applying power to a back-up inverter for any combination of the three main bus inverters in the current power subsystem concept. This detection/switching concept should also be applicable to the two protected bus inverters.

5.8.2 DESIGN DESCRIPTION (Figure 5.8-1)

There are two methods of determining an inverter failure. The first is to check for a low ac output voltage if the input voltage and output current (inverter load) are within specification, and the second is to check for an excessive input current if the output current is not above specification. The "if's" provide protection against external (load) faults which could draw excessive current and drag down the dc (input) voltage.

A comparison voltage from the ac main bus is developed by a transformer and rectifier combination and compared to a reference voltage derived from the dc input. The zener diode in the dc reference line causes the dc comparison voltage to decrease faster than the ac voltage would in the event that the dc bus were being dragged down by an overload. This accomplishes the logic of looking at the ac voltage only if the dc voltage is in spec. The op amp detector provides high gain and current amplification. The second op amp compares the output of a dc current sensor (lin) to a fixed reference to determine excessive input current. The op amp outputs are loaded by a transistor arrangement which simulates a majority vote circuit. A short delay ($\sim$ 1 millisecond) is provided by the capacitor, C6, and the zener diode, CR13, which prevents an output due to a large transient. The filtering in both the voltage and current detection also acts to delay or filter transients. The ac current level detector consists of an ac current transformer, sense resistor, (SBT), a

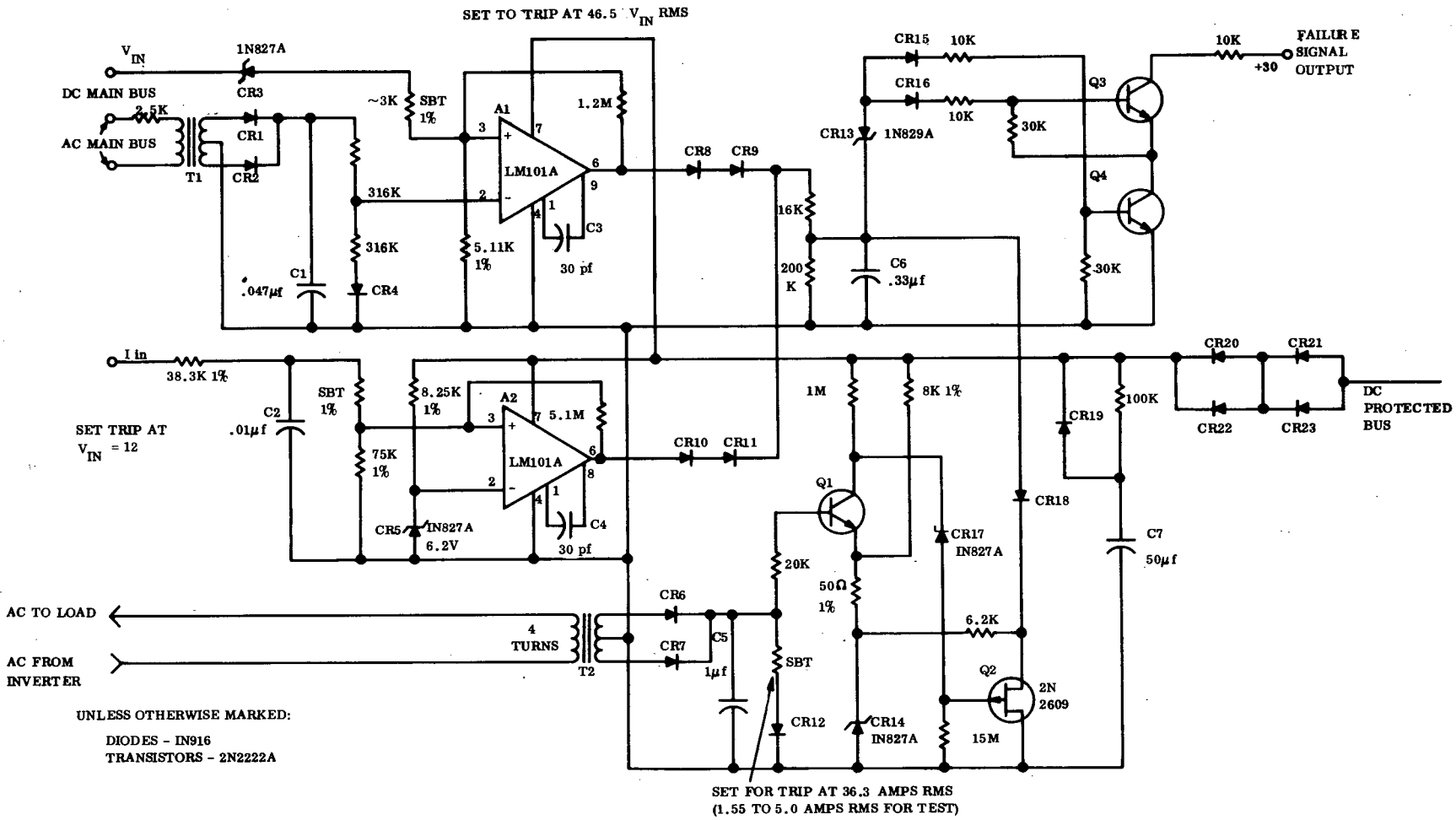


Figure 5.8-1. Level Set Inverter Failure Detector Schematic

reference, and a transistor for the comparator and amplifier. If an overcurrent exists, the transistor, Q1, will be on causing the FET to be on which shorts any op amp output. This accomplishes the logic of looking for a failure only if the output current is under spec limit.

The second way of sensing inverter failures is to check voltages and currents against the inverter turns ratio. That is, the output voltage must be not much less than 5/3 the input voltage, no matter what the input voltage. Likewise, the input current should not be much more than 5/3 the output current.

These ratios, of course, will not hold for voltage at severe overloads, due to high transformer IR drops, nor for current at very light load due to fixed losses in the inverter such as the constant drops in the switching transistor. Figure 5.8-2 presents this design which is preferred due to the fewer piece parts and the greater "accuracy" of the ratio method. The ratio method is capable of detecting smaller degradations in inverter performance than the level method. The op amp (LM101A) provides the needed voltage gain and "floating" inputs which, consequently, are not damaged by differential voltages. However, an op amp requires its inputs to be somewhat above the level of the negative supply to function accurately. Thus, when the voltage or current sense points approach zero, the detector output will be high or low depending entirely on the op amp's input offset characteristics. To compensate for the inverter characteristics and the detector circuit limitations, a bias is used in the voltage detector which causes the detector to "see" more ac than is actually the output of the transformer/rectifier, effectively cutting off the ratio test altogether for very low voltages.

In the current detector, the ratio is precise to within about two amps, so that the bias is applied only when the current falls below about six, (6) amps ac and then sharply cuts off the ratio test to avoid the detector problem of low input voltages.

The remaining section of the circuit is a majority vote capable of sinking five (5) milliamps as the signal to the switch circuit. The role of the failure detector is to decide only when a failure has occurred. The switching circuit contains the logic to determine which inverter is on and to provide the appropriate commands. Each module of the failure detector contains sufficient

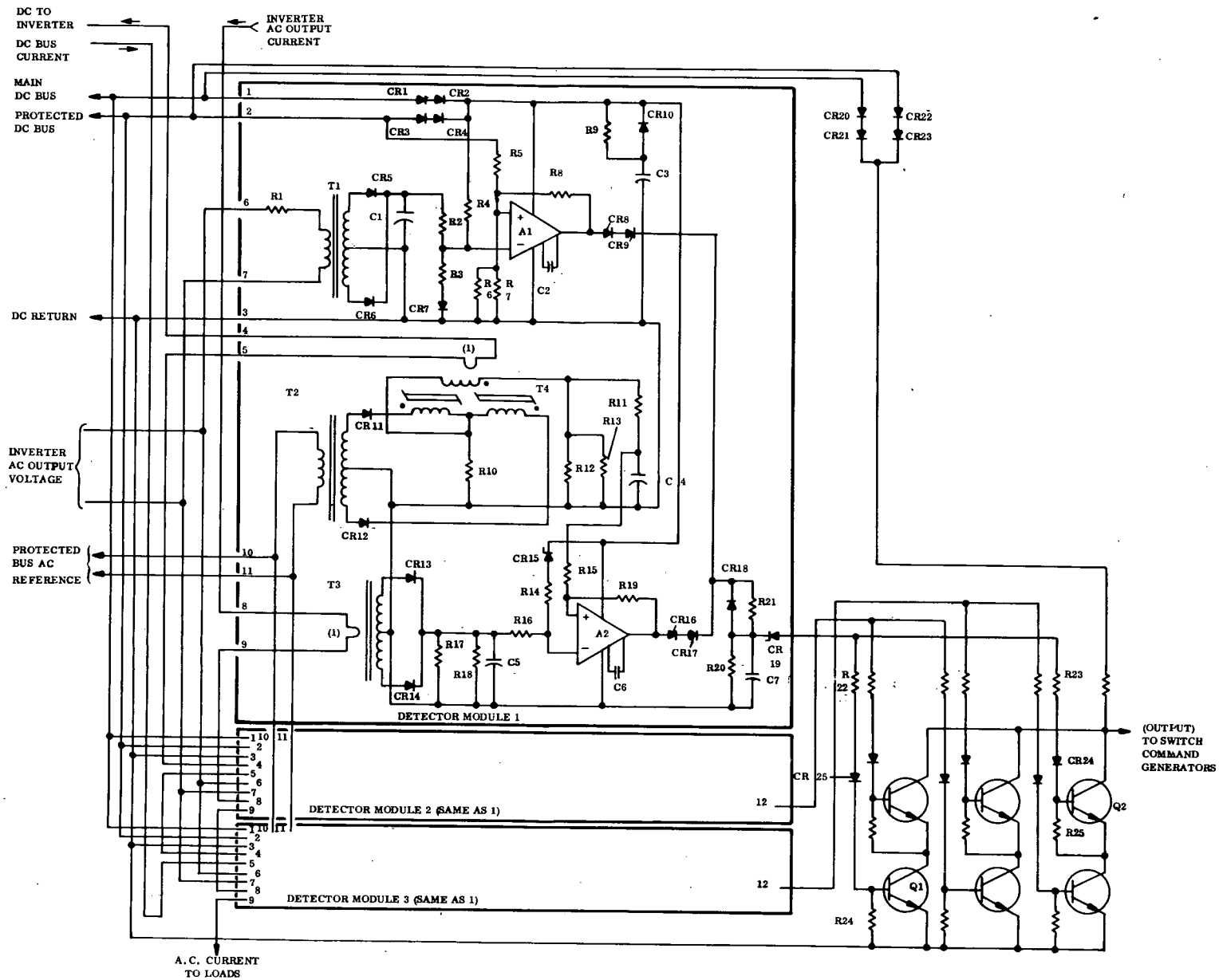


Figure 5.8-2. Inverter Ratio Failure Detector-Qual Unit

energy storage to maintain its output long enough for the switch circuit to switch two, (2) inverters, in the event that the first inverter turned on has failed.

5.8.3 TEST RESULTS

Figure 5.8-3 shows the set-up for the breadboard tests of both units. DC power supplies were used to provide the main bus, the protected bus, the supply to the inverter, and a simulated output of the dc current sensor. In lieu of using the high current and power levels of the actual main inverter, several turns were used around the ac current sensor in order to achieve meaningful results.

For the level detector, the ac input was varied to obtain trip and reset for dc voltages of 24, 26, 28 and 30 volts. The ac current was varied by changing the inverter load to obtain the trip and reset points of the ac overcurrent detector while the dc supply simulating the dc current sensor input was varied to obtain the trip and reset points of the input overcurrent detector. The circuit was tested at -20, 0, 25, 55, and 85^{o}C.

For the ratio failure detector, the voltage trip and reset was determined by varying the ac voltage for different settings of the dc input voltage. The current trips and resets were obtained by varying the supply which simulated the dc current sensor input, for various settings of ac current. The basic unbiased circuit was tested at -20, 0, 25, 55, and 85^{o}C. The same procedure was used in tests at ambient to determine the effects of different biasing schemes.

To obtain the inverter characteristics, special tests were done using a simulated subsystem as shown in Figure 5.8-4. By passing all available current from the simulated power source through the inverter, a worst case characteristic is determined. This extreme overloading produces the lowest ac voltages for a given dc input voltage.

Figure 5.8-5 presents the setup used to test the qual unit failure detector. The inverter, power source, and loading is the same as for the overload test above. The failure detector was added to the inverter and its associated control and supplies. The voltage trips were obtained by overloading the inverter to drag down the dc source also causing reduced ac output. This was done

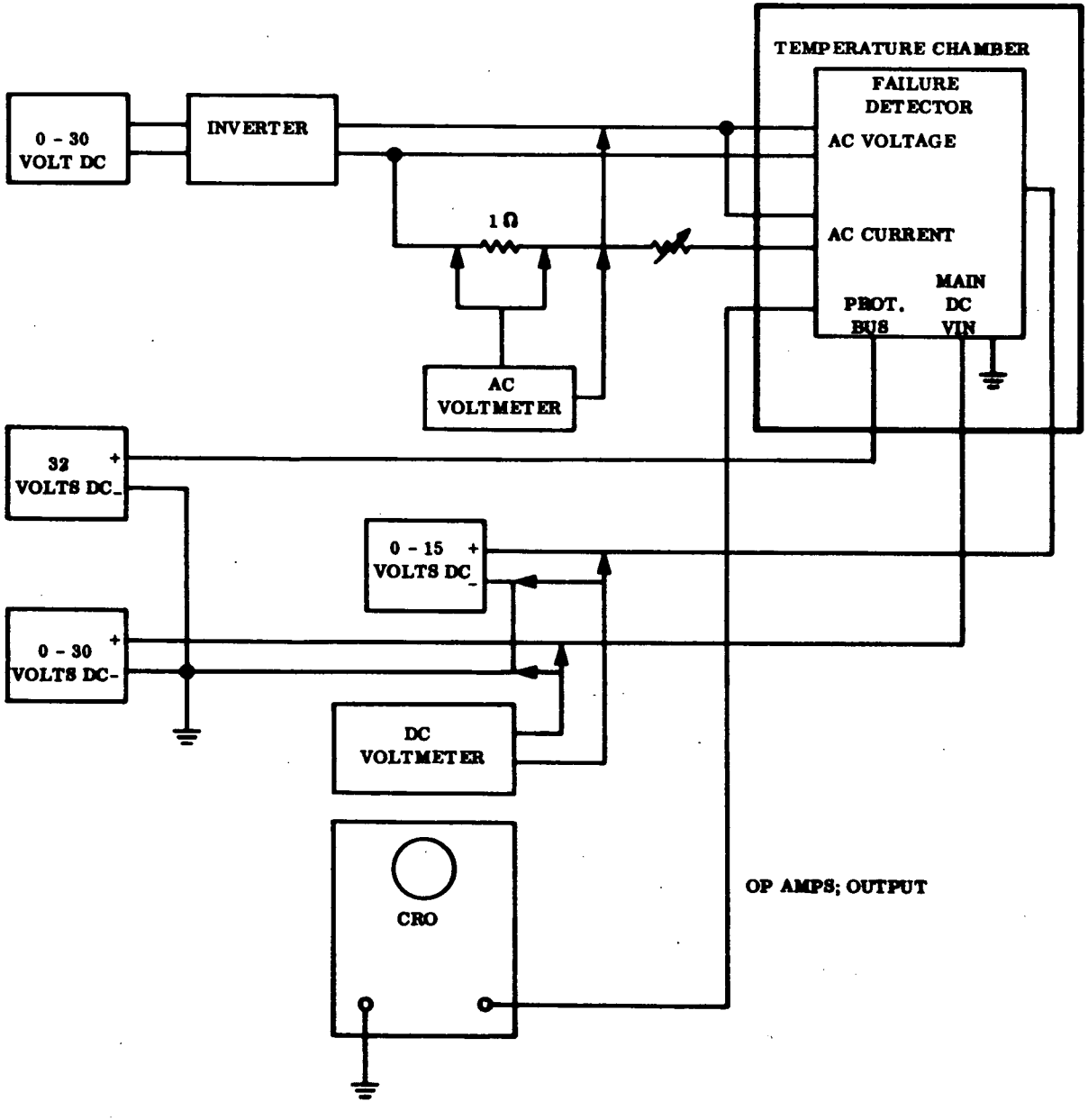


Figure 5.8-3. Inverter Failure Detector Breadboard Test Set-Up

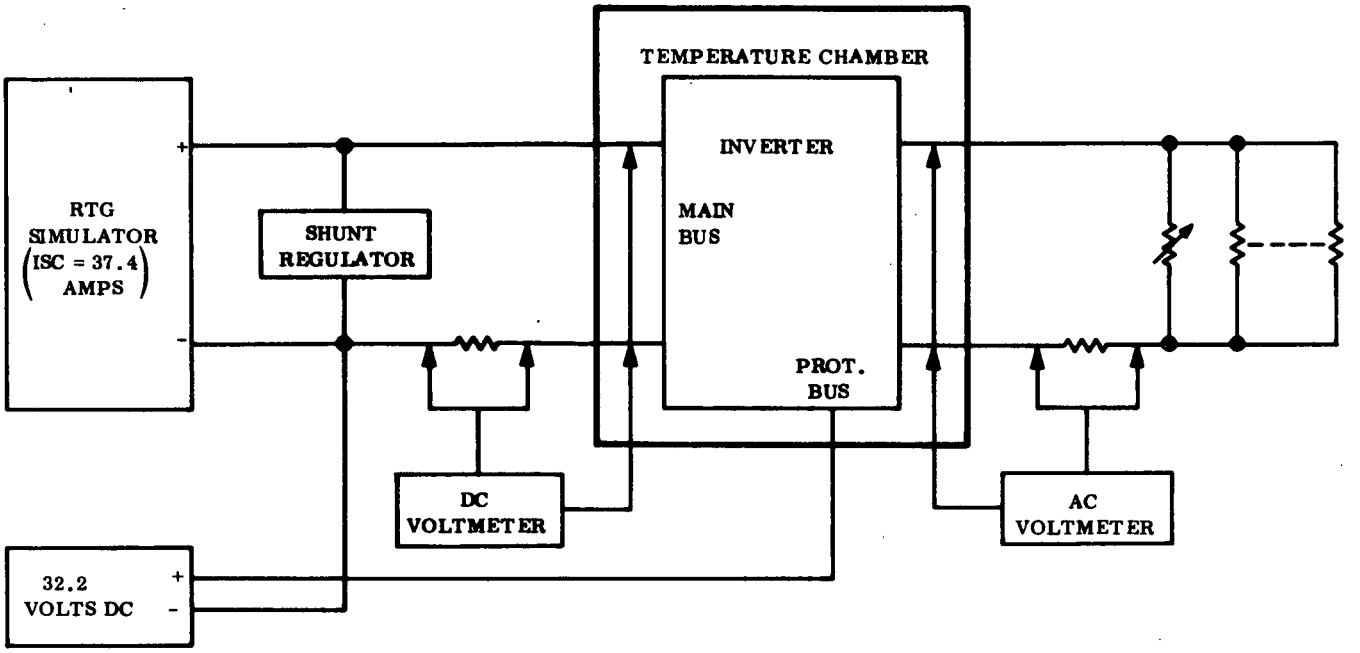


Figure 5.8-4. Power Subsystem Overload Test Set-Up

for many settings of the dc input to the failure detector. The current trips were obtained by setting an ac load, then decreasing R2, which drew extra dc current. The trip and reset of each detector was measured for both voltage and current detectors. These tests were done at -20, 75 and 85°C.

The energy storage capability was checked by connecting the main bus input of the failure detector to the real input bus and disconnecting the protected bus input so that there would be no dc input when the trip was caused by shorting out R2. The resulting dc overcurrent caused the dc bus to go to near zero. The output was monitored on an oscilloscope and a picture taken of the trace to determine the duration of the output. Measurement of the output delay was done in a similar manner. The dc input to the failure detector was set at 30 volts by the external power supply, then the inverter output was shorted to simulate an ac undervoltage. A picture was taken of the three voltage detector outputs and the failure detector output. These tests were conducted at -20, 0, 25, 55, and 85°C.

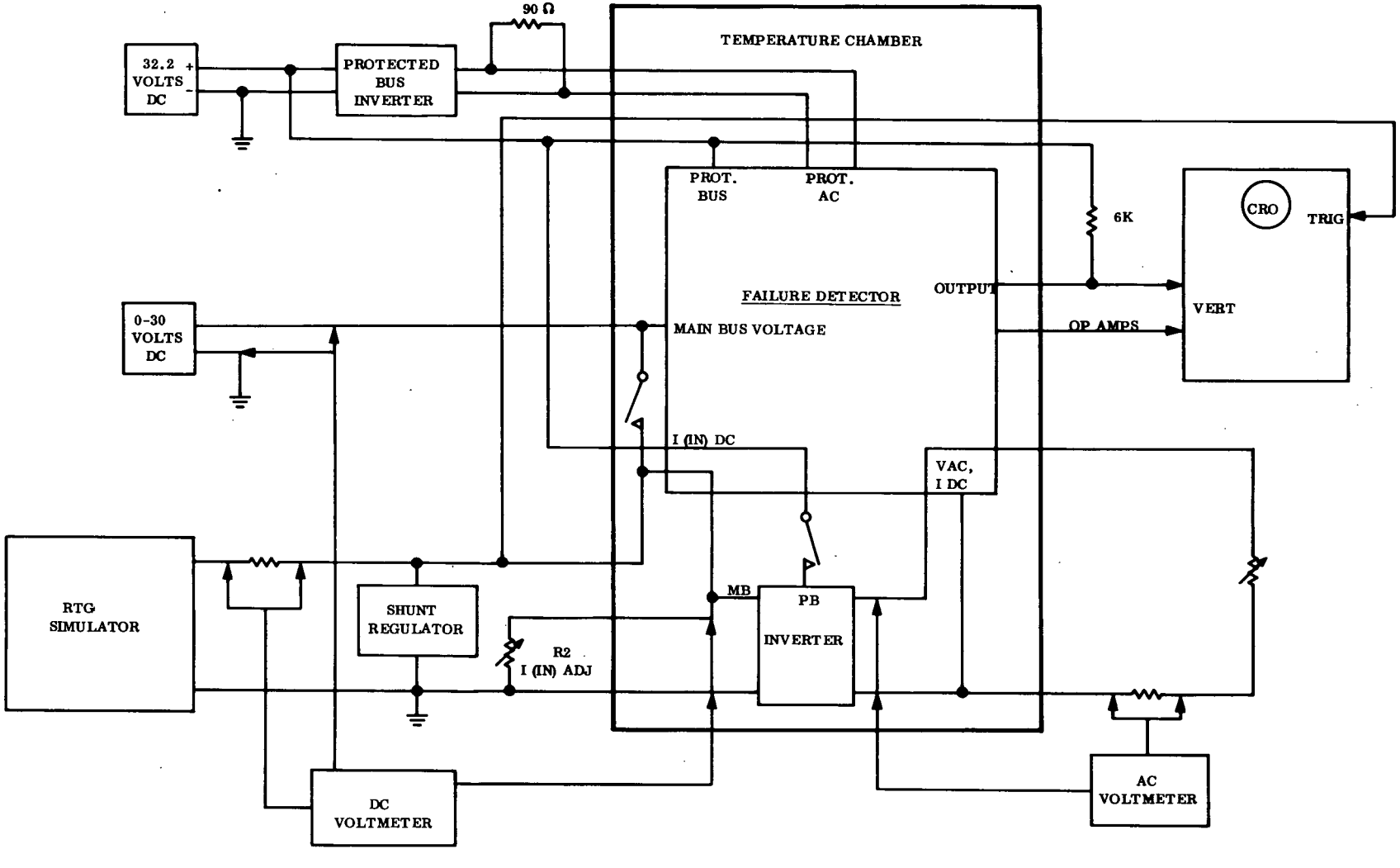


Figure 5.8-5. Inverter Qual Failure Detector Test Set-Up

5.8.3.1 Level Detector Results

Figure 5.8-6 presents the trip results for the level detector breadboard. The current trips include the scaling, so they correspond to the actual currents that would occur in a real setup. Figure 5.8-7 shows how the voltage trip responds to changes in the dc voltage. Figure 5.8-8 shows the output delay and the energy storage capacity.

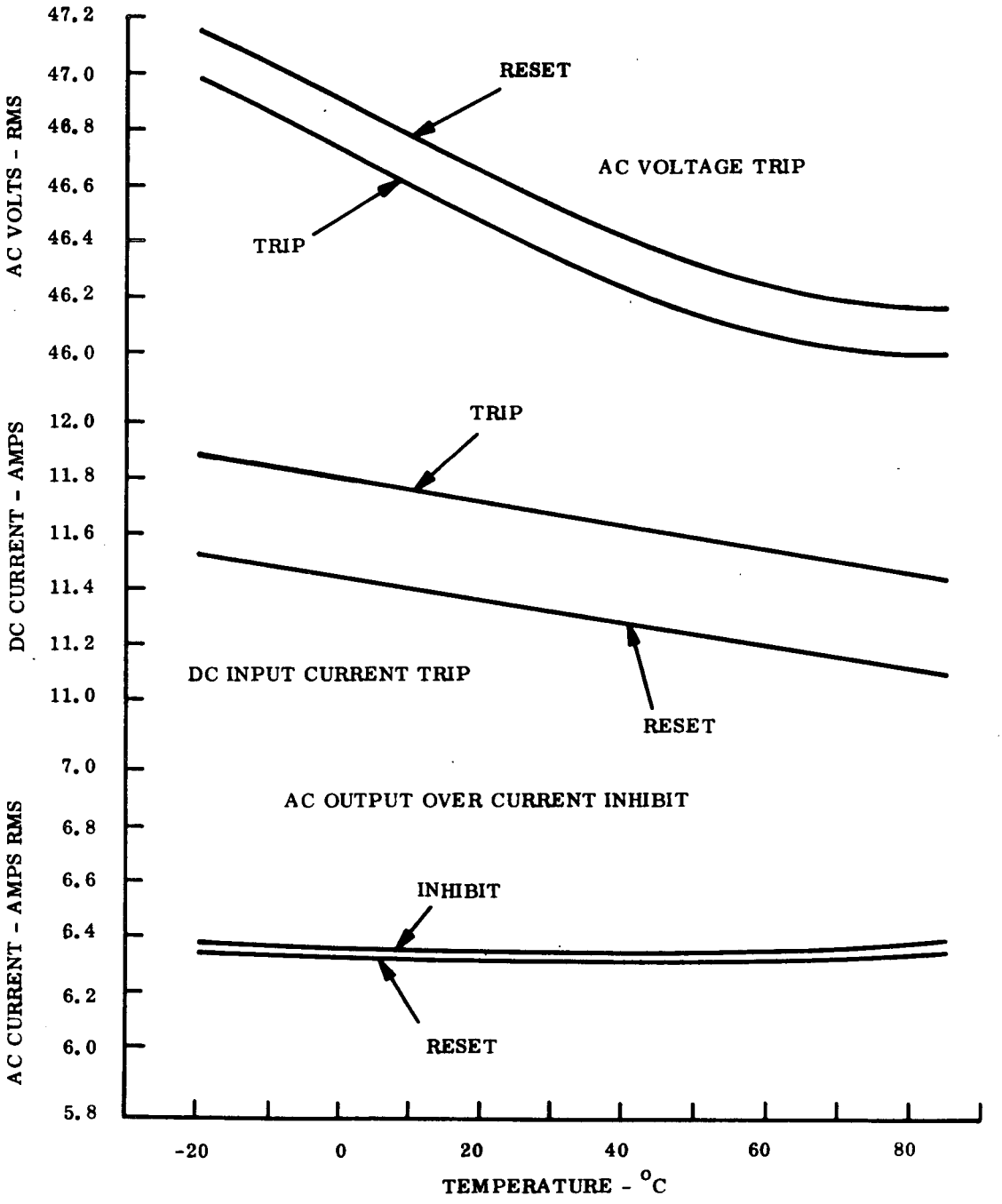


Figure 5.8-6. Inverter Level Failure Detector Trips

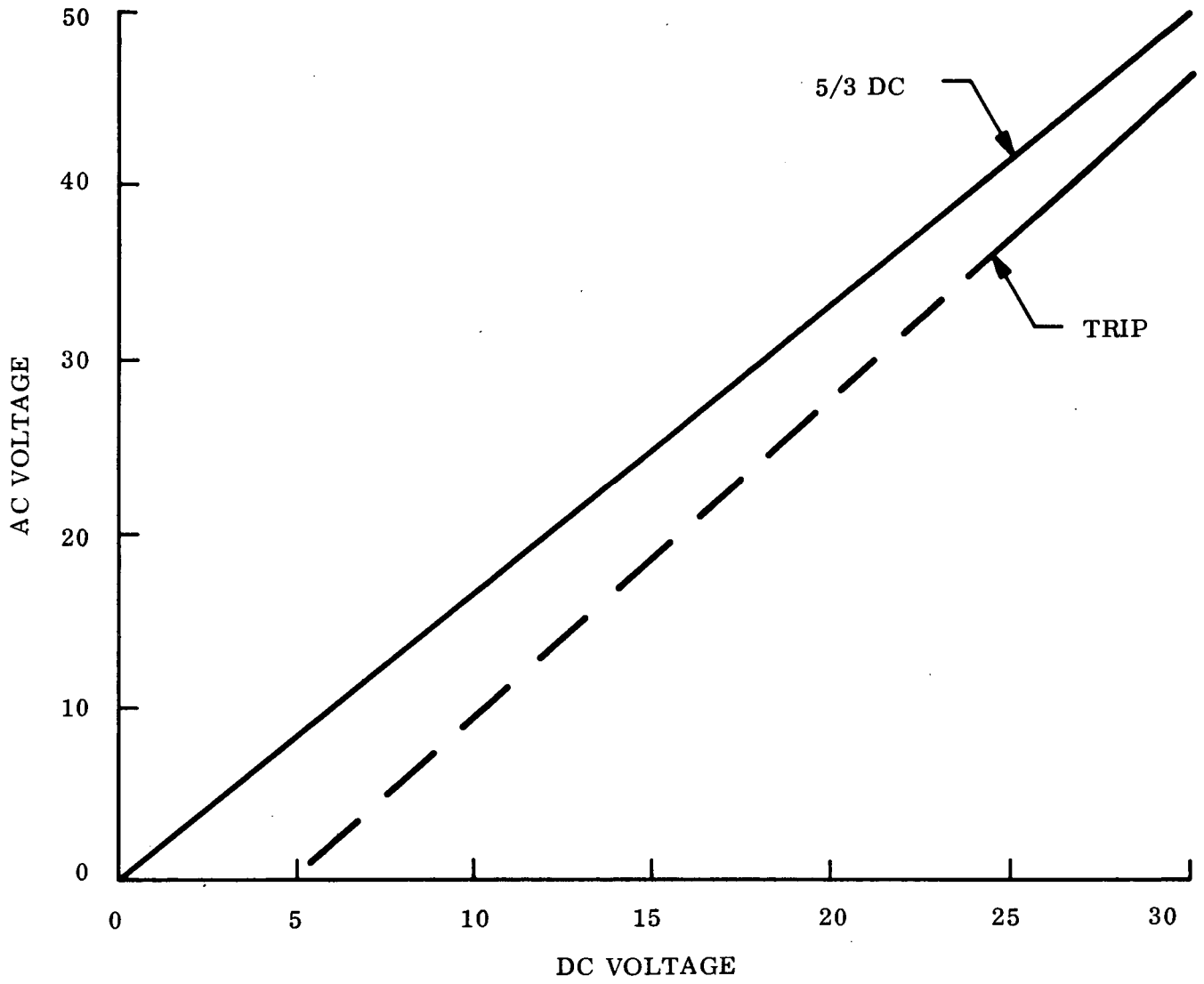


Figure 5.8-7. Inverter Level Failure Detector Voltage Trip AC/DC Relationship

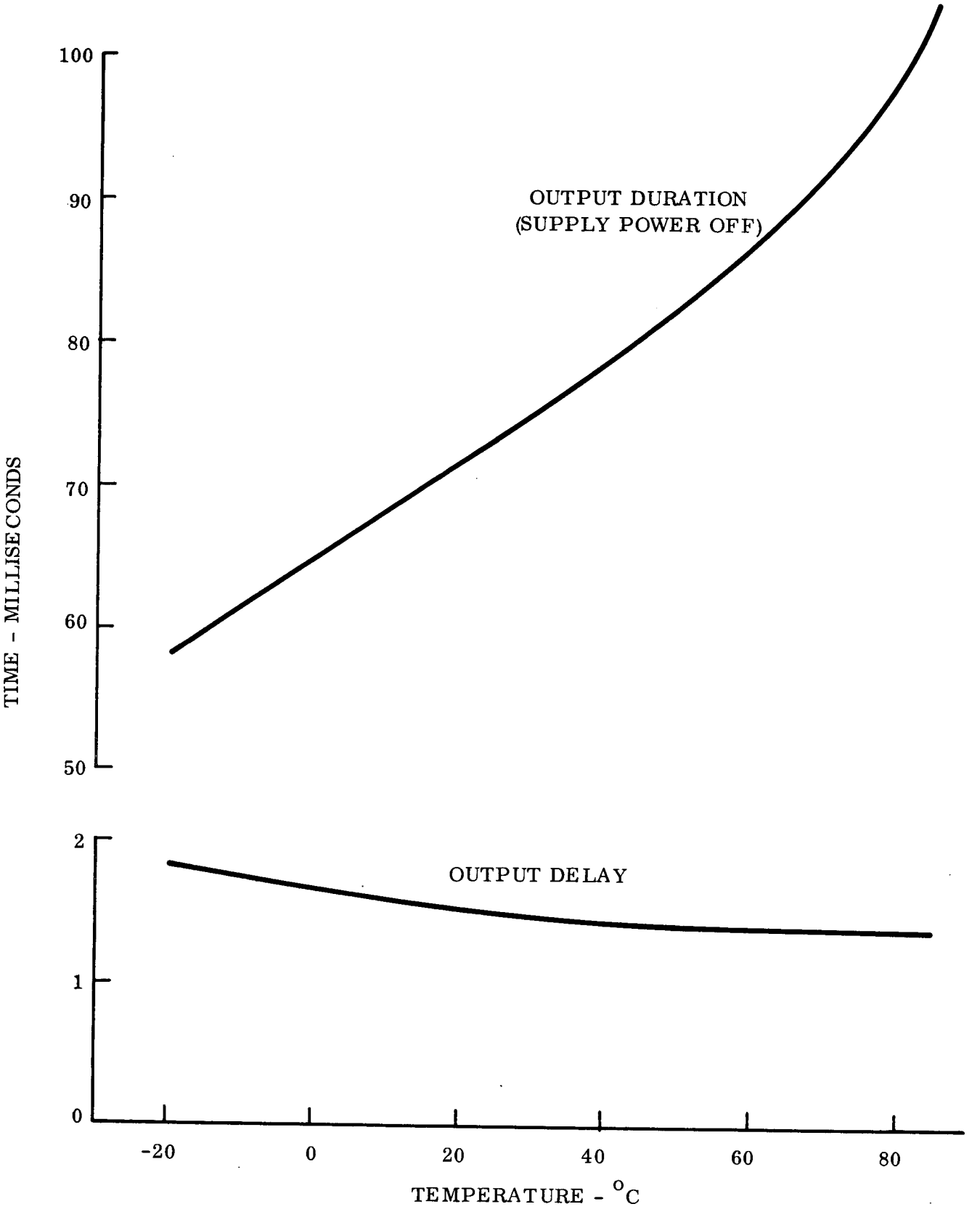


Figure 5.8-8. Inverter Level Failure Detector Output Delay and Energy Storage Duration

5.8.3.2 Subsystem Configuration Results

Figure 5.8-9 presents the voltage results of the simulated bus tests, passing all available current through the main inverter. Figure 5.8-10 shows the current results. Figure 5.8-11 shows the transfer function of the current sensors which were tested simultaneously with the bus tests.

The dc sensor was designed to fall off before the ac sensor to preclude erroneous trip of the current ratio detector at high currents due to sensor non-linearity.

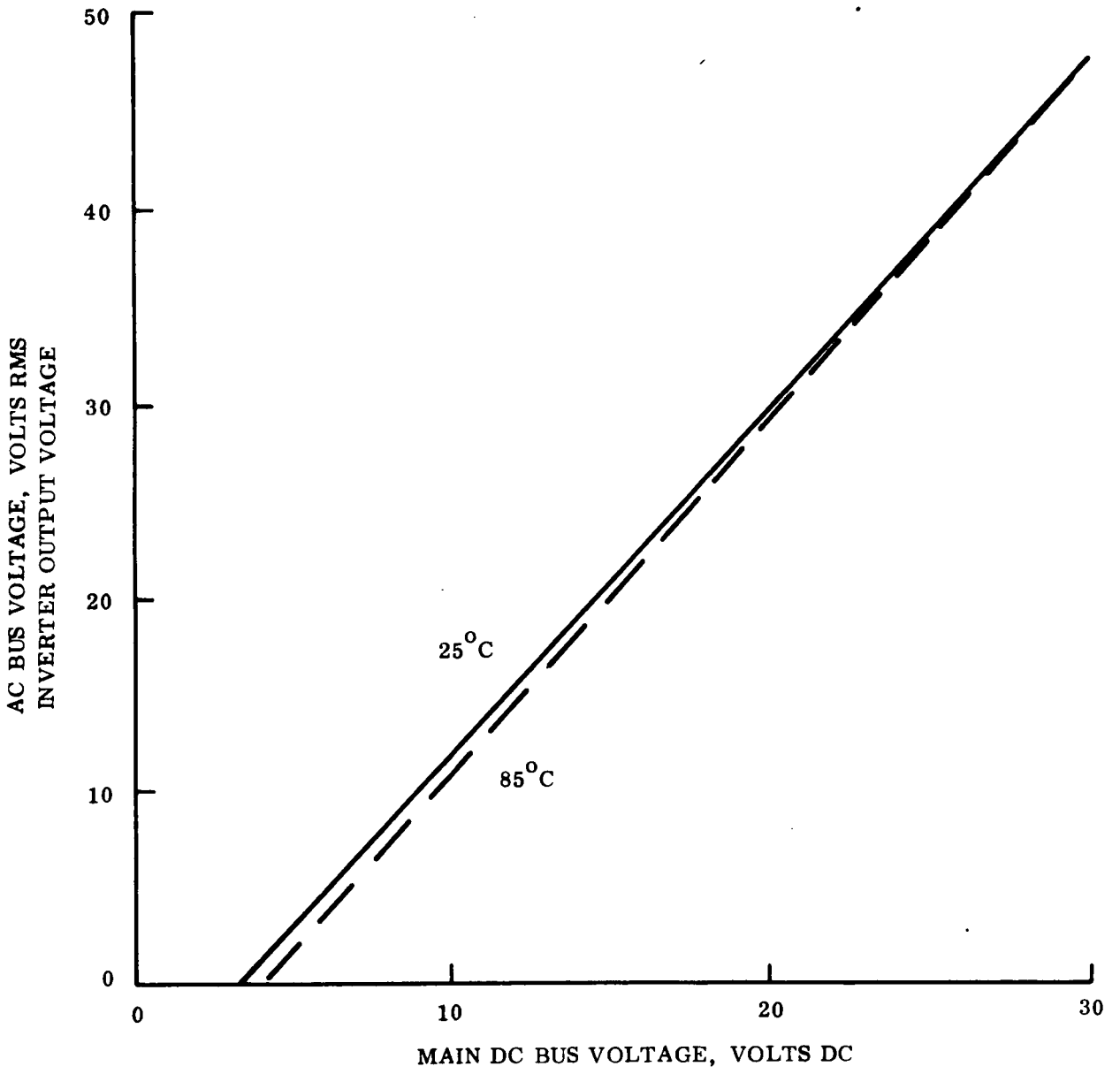


Figure 5.8-9. Power Subsystem AC Bus Overload Voltage Characteristics (Qual Unit Main Inverter, ~37.4 Amps DC Short Circuit)

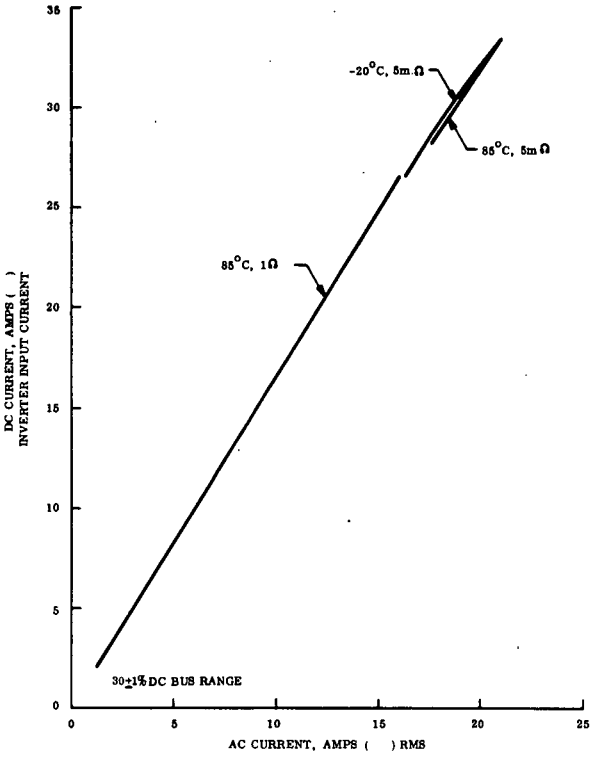


Figure 5.8-10. Power Subsystem AC Bus Overload Current Characteristics

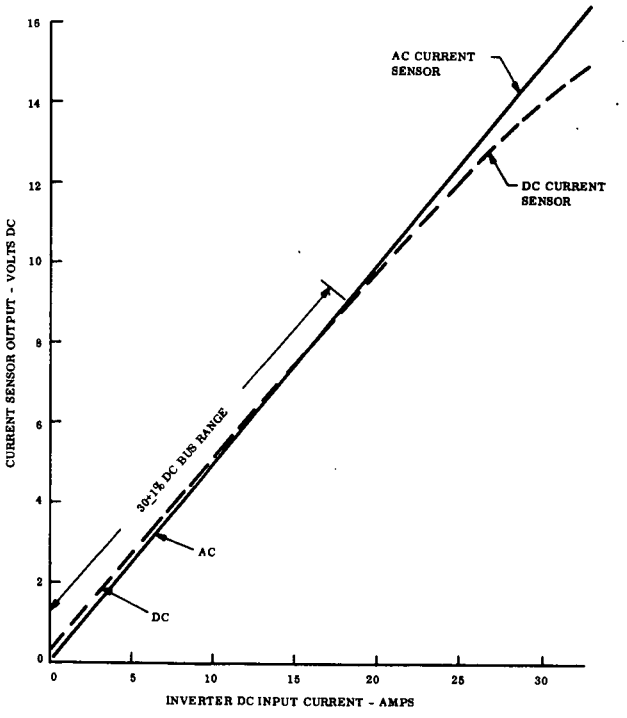


Figure 5.8-11. Failure Detector Current Sensors Linearity (Qual Unit Main Inverter - DC Input and AC Output

5.8.3.3 Ratio Detector Results

Figures 5.8-12 and 5.8-13 show the results for unbiased ratio detectors. The dashed line on the voltage curve is the inverter true characteristic. The current curve shows the effect of the detector offset at low input voltage.

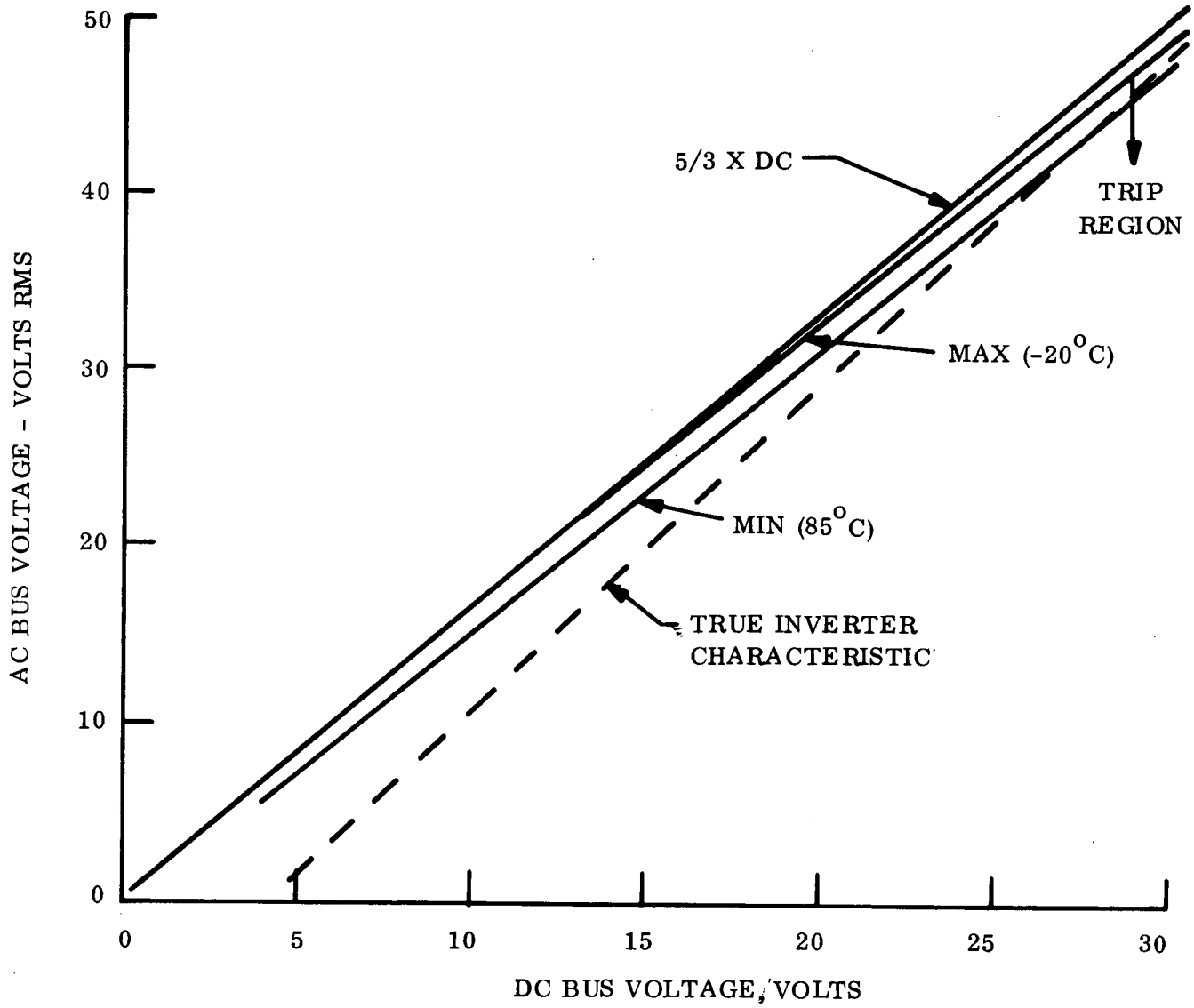


Figure 5.8-12. Ratio Failure Detector Voltage Trip

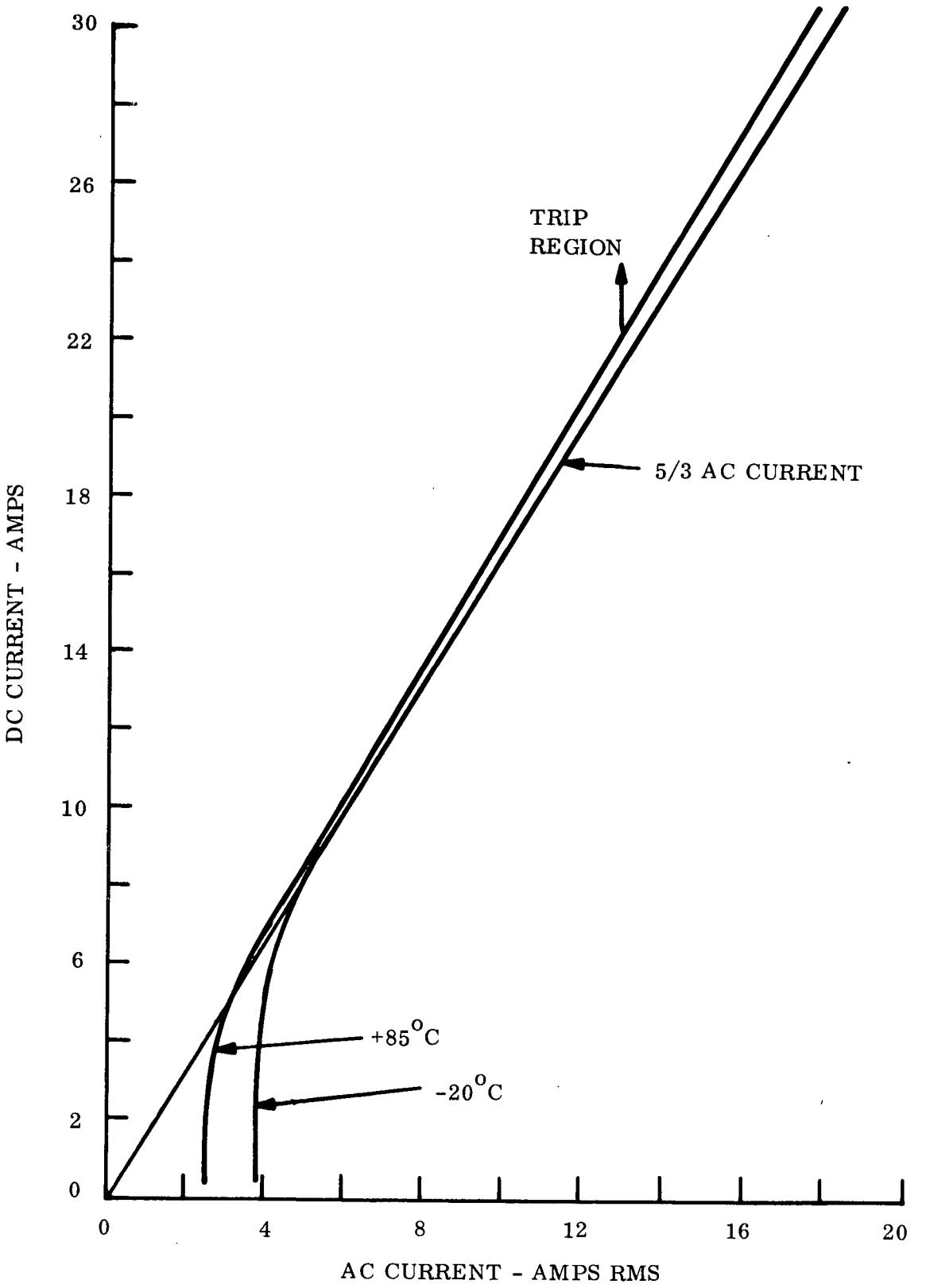


Figure 5. 8-13. Ratio Failure Detector Current Trip

The scaling is three (3) dc amps per volt. Figure 5.8-14 shows the schematic of the biased ratio detector. R1 and Z1 bias the voltage detector while R2 and Z2 bias the current detector. To aid the current detector low voltage problem, the scaling was changed to two (2) dc amps per volt.

Figure 5.8-15 shows the effect of bias in the voltage detector.

Figure 5.8-16 shows the effect with no zener. Using a 12-volt zener, the same effect can be obtained with just a resistor because the zener is always on. Using a higher breakdown voltage (2 zeners) produces a break, as seen in Figure 5.8-17. The basic current detector and inverter characteristics are too precise to need biasing over a wide range as is needed in the voltage detector to change the overall slope of the curve. Therefore, a break is all that is needed to prevent an erroneous output when the currents get low, and the qual unit design uses a high breakdown voltage and low resistance to "break off" the current ratio measurement at low currents. This also prevents any problems from a dc current sensor with a high zero current offset, which would cause high output at low currents.

5.8.3.4 Qual Unit Failure Detector Results

Figure 5.8-18 presents the results, including all temperatures for the current trip function. While the graph of lowest reset appears to touch the actual curve, actually it does not because resets were always obtained without fully opening R2 to infinity. The ac voltage measured across the 5 milliohm shunt is not linear with current when checked against the 1Ω shunt. In performing the test, it is also impossible to keep the ac current setting, when changing R2 to obtain detector reset, if operating beyond the range of bus regulation (above 18 amps dc). In operation, the current trips functioned correctly. Figure 5.8-19 presents the voltage trip results. In correlating the measured bus characteristics and the ratio detector biasing results, insufficient bias was selected for the qual unit design. It seems evident, though, that proper biasing would produce the desired results. Figure 5.8-20 provides a better analysis of the trip function. As seen, there is only a slight adjustment of the slope of the trip function (bias) to push the trip and resets below the actual inverter characteristic. The trips and resets must fall below the dotted line of Figure 5.8-20. Point A shows where the resets began to just exceed the actual bus voltage. To check the effect of inverter loading on the results, the protected bus input of 2.8 amps was removed for an 85°C test and the results

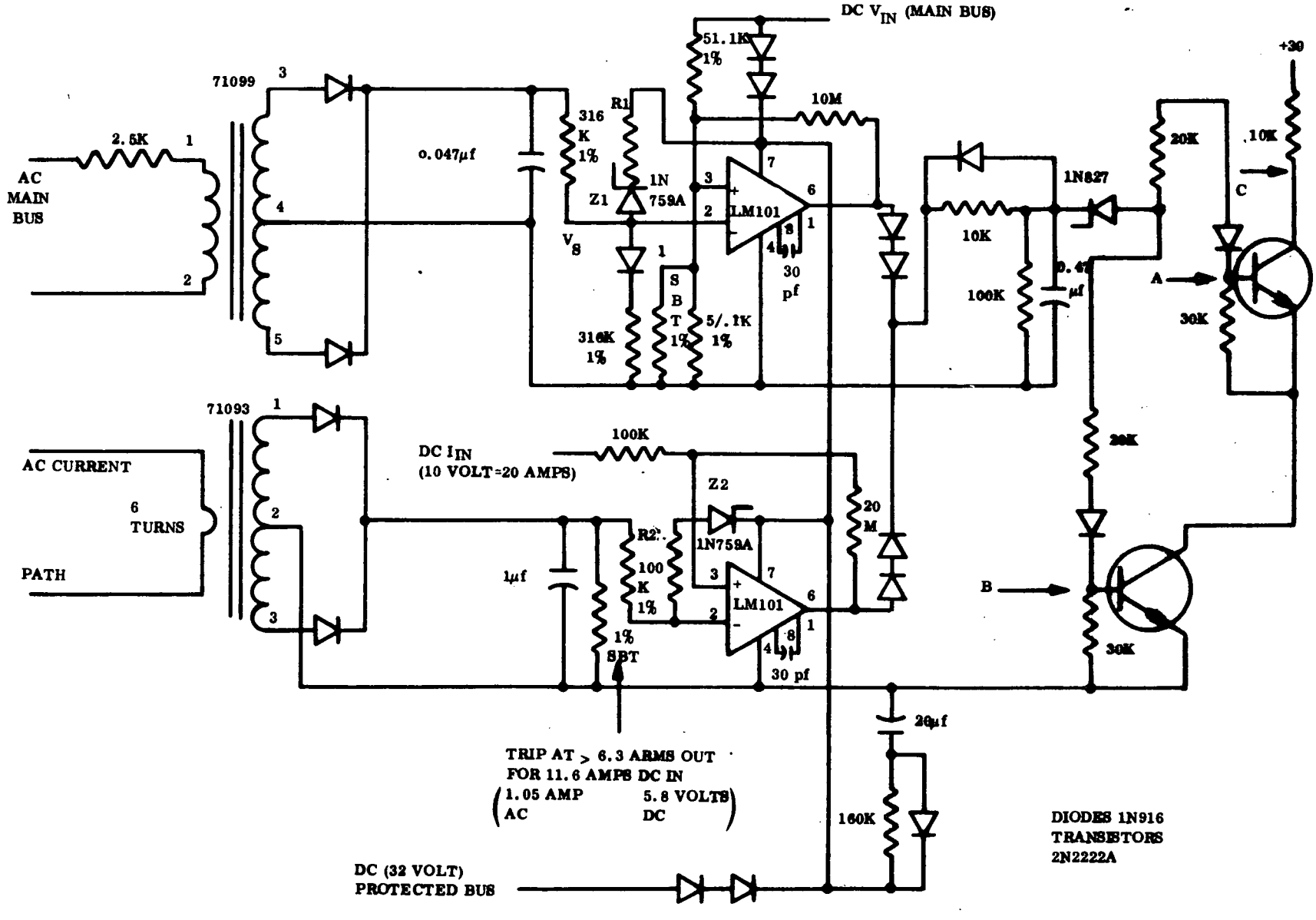


Figure 5.8-14. Ratio Failure Detector Schematic

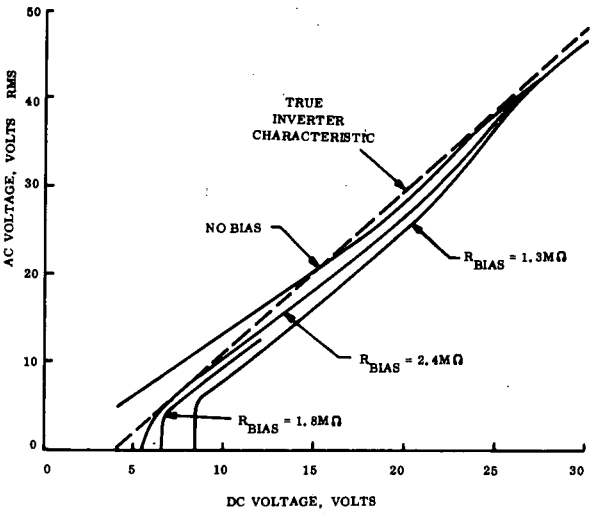


Figure 5.8-15. Biased Ratio Failure Detector Trip Function (Resistor-Zener Bias)

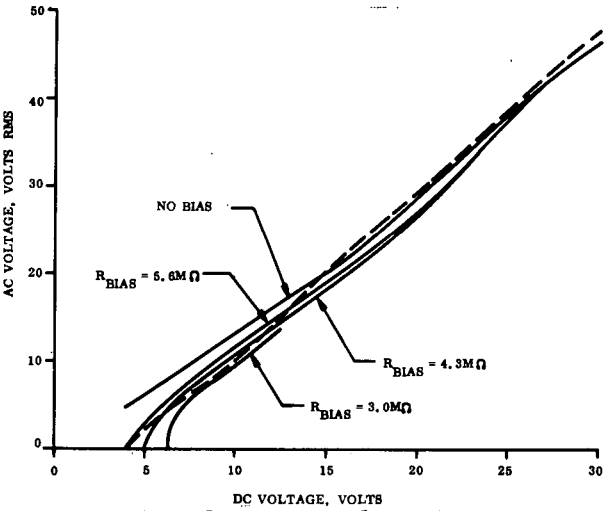


Figure 5.8-16. Biased Ratio Failure Detector Trip Function (Resistor Bias)

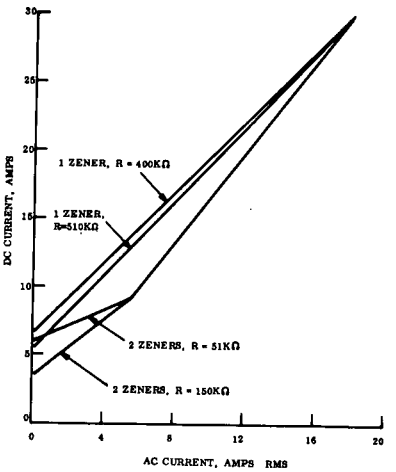


Figure 5.8-17. Biased Ratio Failure Detector Trip Function (Resistor-Zener Bias)

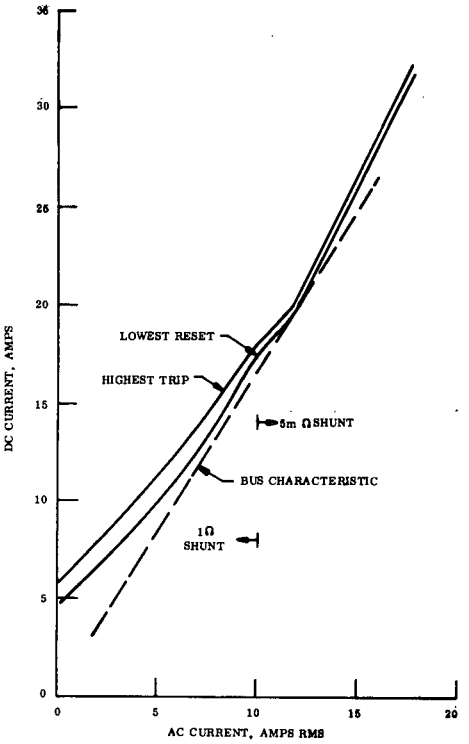


Figure 5. 8-18. Qual Unit Failure Detector Current Trip

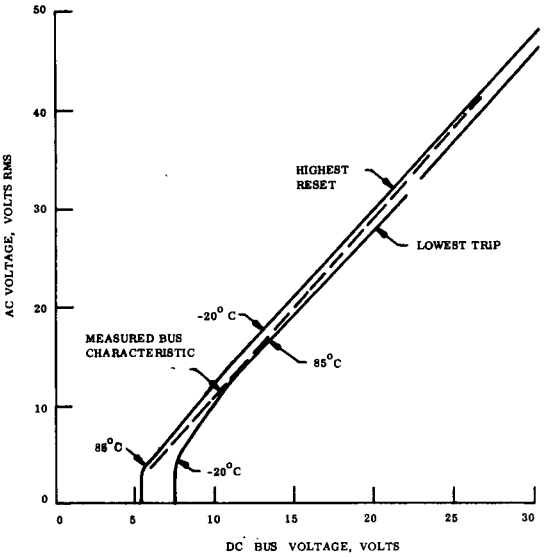


Figure 5. 8-19. Qual Unit Failure Detector Voltage Trip

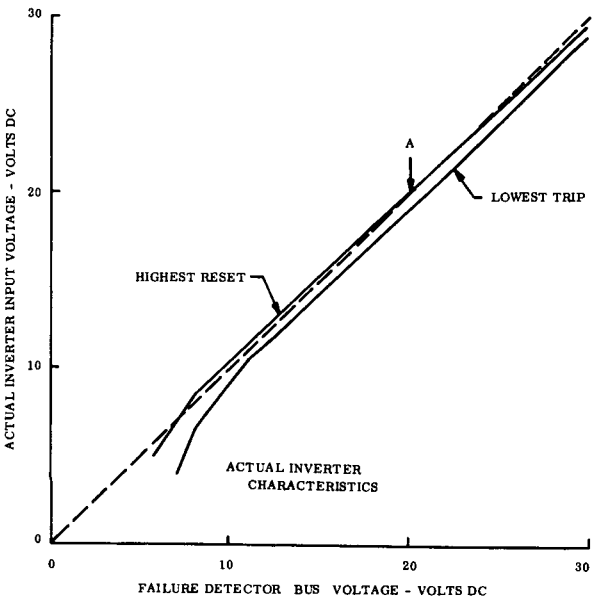


Figure 5. 8-20. Qual Unit Failure Detector Voltage Trip DC Voltage Comparison

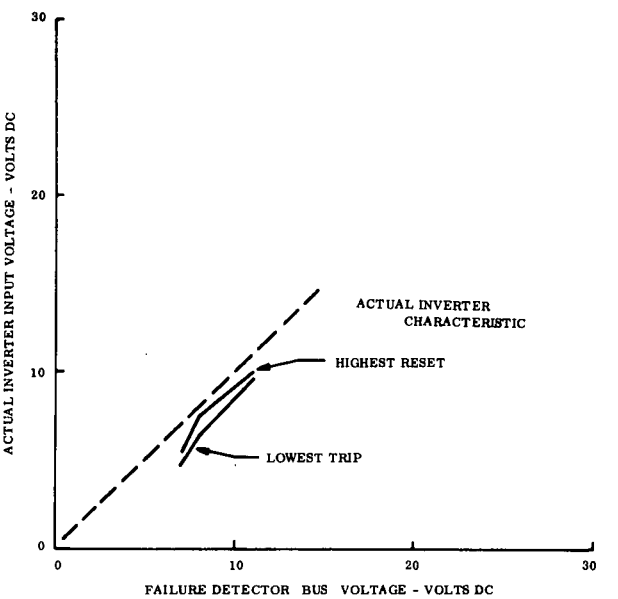


Figure 5. 8-21. Qual Unit Failure Detector Voltage Trip Reduced Loading at 85°C

are shown in Figure 5.8-21. Even at a large overload dragging down the dc bus, the inverter ac output voltage is sensitive in the range of three amps less the output current. If close accuracy is desired, the detector should be designed to "just" work correctly with the inverter heavily overloaded as tested. The margin will be provided by the presence of dc loads and RTG degradation through the mission. If such accuracy is not desired more margin could be put into the trip point at thirty (30) volts and more biasing may not be required.

Figure 5.8-22 shows the output delay and energy storage results. Output duration in excess of 30 milliseconds should assure sufficient time to switch 2 inverters, so the design is adequate. The output delay is to provide protection against transients; without knowledge of these transients it is impossible to say the results show sufficient delay. The total delay was always greater than 500 microseconds from the start of the transient (in this case, shorting the inverter output) due to additional delay in the voltage detector filtering. The same would be true due to current transducer filtering, so in general there seems to be sufficient transient immunity.

5.8.3.5 Flight Design Considerations

The proper biasing and trip setting for the voltage must be tested following further definition of requirements. Further subsystem development test results should be studied to determine transient characteristics. The failure detector must be tested with the switching circuit in the subsystem testing.

5.8.4 FAILURE MODE, EFFECT, AND CRITICALITY ANALYSIS

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown in Table 5.8-1. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

5.8.4.1 Specific Recommendations

Both the Protected Bus and Main Bus Inverter Failure Detectors use the 2N2222A transistors in the majority voting circuit. To provide for the possible 41 vdc transient overvoltage due to an open circuit failure of the Current Throttle, it is recommended that the 2N2222A transistor with a a V_{CEO} of 40 volts be replaced by a transistor with a V_{CEO} of 60 volts or higher.

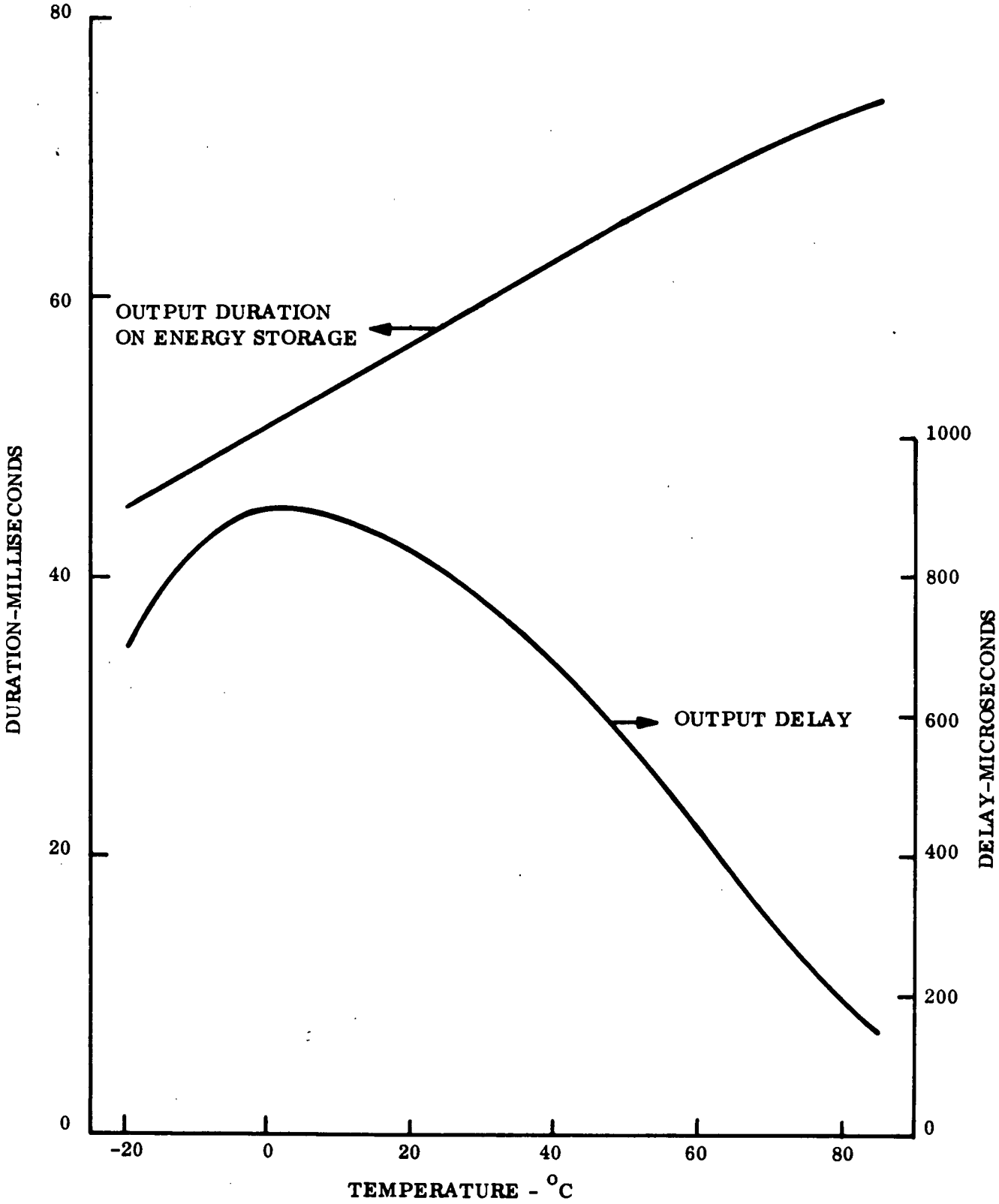


Figure 5.8-22. Qual Unit Failure Detector Output Delay and Energy Storage Duration

5.8.4.2 Main Inverter Failure Detector/Switch Command Generator-Timing Problem

In the course of analyzing the circuitry of the Main Inverter Failure Detector and the Switch Command Generator that receives the failure detector signal, it was discovered that the capacitor C7 (see Figure 5.8-2) discharge time constant is relatively long. This implies that the output signal indicates an inverter failure after the failure has been corrected because it takes the capacitor some time to discharge.

The condition is this:

1. The failure detector had sensed an inverter failure and caused the No. 1 switch command generator to turn off the No. 1 inverter and turn on the No. 2 inverter.

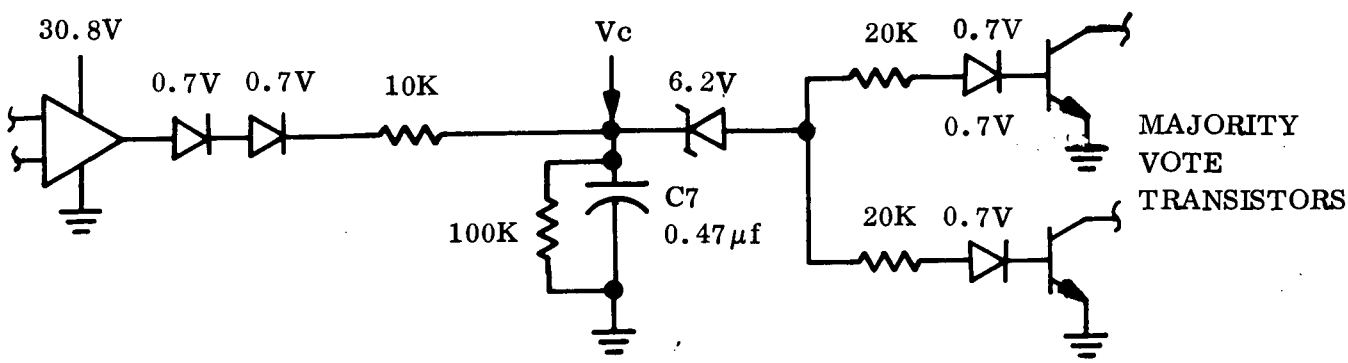
2. The No. 2 inverter comes on and the input signals to the failure detector return to spec, but the output still indicates a failure since the capacitor, C7, has not discharged sufficiently.

3. The same switch that turns on the No. 2 inverter, also turns on the No. 2 switch command generator. When the No. 2 switch command generator receives a failure signal from the failure detector, it turns off the No. 2 inverter and turns on No. 3.

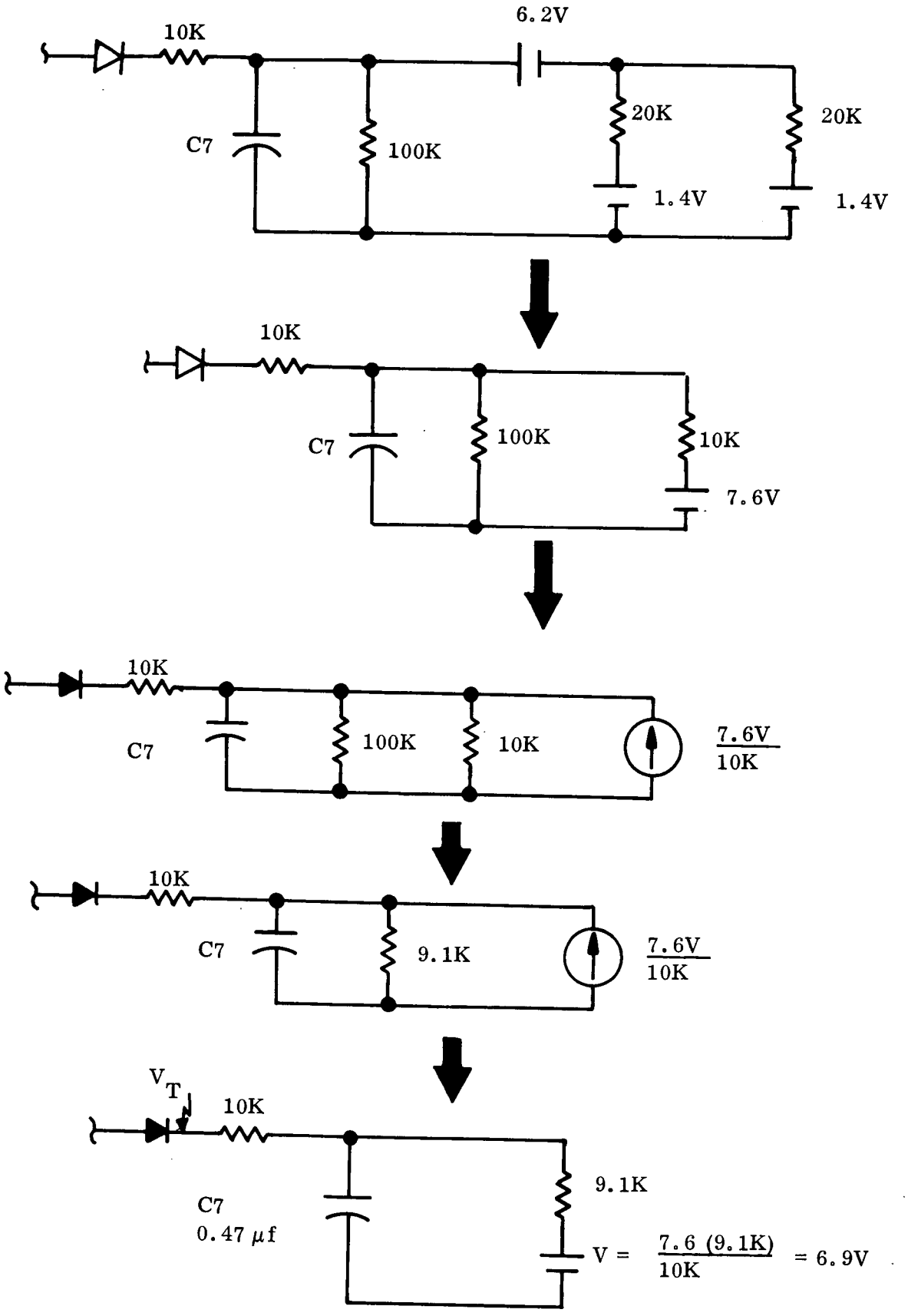
4. There is a delay in response to a failure signal built in the No. 2 switch command generator. If the failure signal stops before this time delay expires, there would not be a problem switching off a good No. 2 inverter and going to the No. 3 inverter.

An investigation of these timing relationships follows:

The failure detector circuitry from the output of the op amp to the transistors in the majority vote circuit is as follows (see Figure 5.8-2):



The charge/discharge circuit for the capacitor is:



When the op amp sensed the failure of the No. 1 inverter, the output went to about 2 volts below the supply voltage of 30.8 vdc (Protected Bus voltage of 32.2 minus two diode drops), so the op amp output is 28.8 vdc. V_T is two more diode drops below or 27.4 vdc.

When V_T is 27.4 vdc, the steady state voltage across the capacitor is found to be:

$$\begin{array}{r} 27.4 \\ -\ 6.9 \\ \hline \end{array}$$

20.5 vdc, which will be dropped across the two resistors.

The voltage drop across the 10K resistor is:

$$\frac{10K \quad (20.5\ V)}{19.1K} = 10.7\ V$$

The capacitor voltage will be:

$$27.4 - 10.7 = 16.7 \text{ vdc}$$

The discharge time constant is:

$$T1 = RC7 = (9.1 \times 10^{3})\ (.47 \times 10^{-6}) = 4.28 \text{ ms}$$

And it is discharging from 16.7 to 6.9 V,

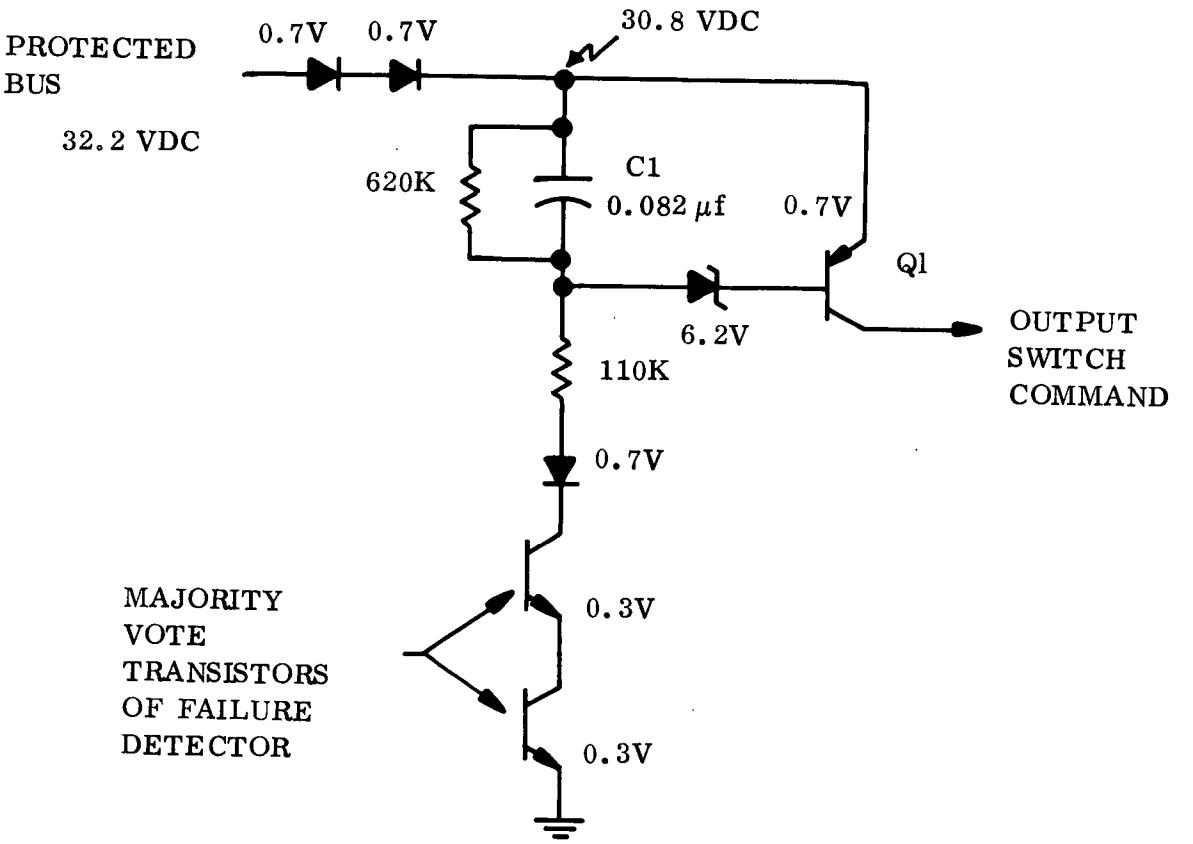
$$\text{or} \quad \frac{6.9}{16.7} = 41.3\% \text{ discharge}$$

This takes 0.88 T1 or 0.88 x 4.28 ms

$$= 3.78 \text{ ms}$$

Thus, the majority voting transistor turns off 3.78 milliseconds after the inputs to the failure detector have returned to spec.

The circuit that receives the failure detector signal is (see Figure 5.7-1):



When the voltage across C1 exceeds 6.9 vdc, Q1 turns on and issues the "Switch Inverter Commands".

The final voltage on the fully charged capacitor is:

$$\frac{620}{730}\left[30.8 - (.7 + .3 + .3)\right] = \frac{62}{73}\left[30.8 - 1.3\right] = \frac{62}{73}\ (29.5)$$

$$= 25 \text{ vdc (If it were not restricted by the zener and } V_{BE} \text{ drops).}$$

Now:

$$\frac{6.9\ V}{25\ V} = 27.6\%$$

The time required to charge 27.6% is

$$0.322\ T$$

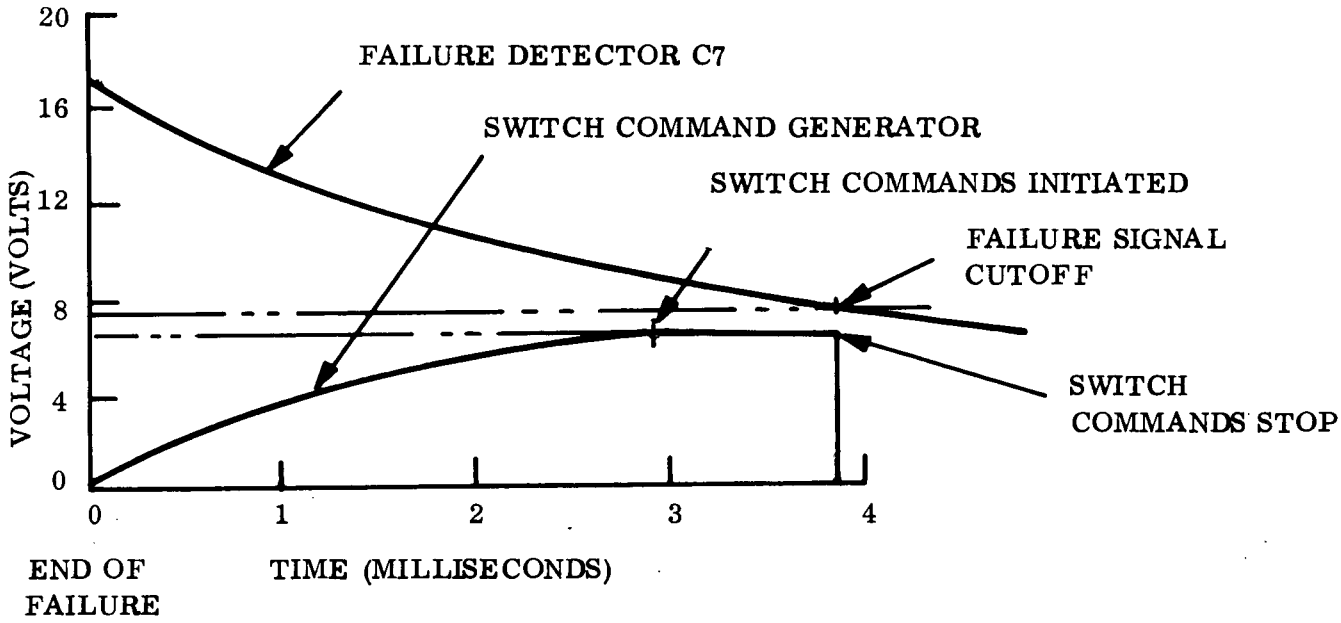
$$T = (0.082 \times 10^{-6})\ (110 \times 10^{3}) = 9.02\ ms$$

and

$$0.332 \times 9.02\ ms = 2.9\ ms$$

Hence, 2.9 ms after being powered on, the No. 2 inverter switch command generator will be activated by the failure detector and remain on for 0.88 milliseconds.

The charging/discharging of the two capacitors is shown below:



This discharge time of the inverter failure detector capacitor C7 must be shortened such that the failure signal stops approximately 1 millisecond or less after the input signals to the failure detector return to normal and indicate that the inverter is operating properly.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	R1	Resistor	Attenuates transients which occur at each half cycle of the A.C. reference also current limits the inverter output voltage measurement in the event of a short in the sensing circuitry.	Open		Loss of inverter output voltage measurement. Inverting input to A-1 Op Amp goes low causing output to go high.			Failure detector #1 will remain inoperative.
2	R2	Resistor	Part of the voltage divider which samples the recified inverter output voltage.	Open		Inverting input of the A1 Op Amp goes low causing the output to go high.			Failure detector #1 will remain inoperative.
3	R3	Resistor	Part of the voltage divider which samples the recified inverter output voltage.	Open		Inverting input of the A1 Op Amp goes high. Output will remain low.			Failure detector #1 can't sense voltage failures. Can still sense current failures.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
4	R4	Resistor	Biases the A.C. voltage such that the voltage comparison is not made at very low input levels	Open		Inverting input of the A1 Op Amp goes low, causing the output to go high.			Failure detector #1 will remain inoperative.
5	R5	Resistor	Part of the voltage divider which samples the inverter input voltage	Open		Non-inverting input of the A1 Op Amp goes low, causing the output to remain low.			Failure detector 1 can't sense voltage failures. Can still sense current failures.
6	R6	Resistor	Part of the voltage divider which samples the inverter input voltage	Open		Non-inverting input of the A1 Op Amp goes high, causing the output to go high.			Failure detector #1 will remain inoperative.
7	R7	Resistor	Part of the voltage divider which samples the inverter input voltage	Open		Non-inverting input of the A1 Op Amp goes high, causing the output to go high.			Failure detector #1 will remain inoperative
8	R8	Resistor	Feedback which determines the reset level of the voltage detector after having been tripped.	Open		No hysteresis. Op Amp output oscillation could occur if inverter output voltage was right at the trip point.			Failure detector #1 would not be effective for identifing small voltage failures.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
9	R9	Resistor	Limits the charge current into energy storage capacitor C3.	Open		C3 will not provide energy to operate failure detector #1 in the event of an undervoltage of the D.C. buses (Main & Protected)			
10	R10	Resistor	Feedback to provide Mag Amp linearity	Open		The output of the current sensor will go high because the voltage developed on the secondary of T2 will be dropped across R12-R13. This high input to non-inverting input of A-2 Op Amp causes the output to go high.			Failure detector #1 would remain inoperative.
11	R11	Resistor	In conjunction with C4 acts to filter switching transients.	Open		Loss of inverter input current measurement causes the A2 Op Amp output to go high.			Failure detector #1 will remain inoperative.
12	R12	Resistor	Converts the DC current measurement into a voltage level	Open		Voltage level goes high. Results in a high output of A2 Op Amp.			Failure detector #1 will remain inoperative.
13	R13	Resistor	Converts the DC current measurement into a voltage level	Open		Voltage level goes high. Results in a high output of A2 Op Amp.			Failure detector #1 will remain inoperative.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
14	R14	Resistor	Biases the inverter output current sense point to cut off the current comparison at low current levels.	Open		Inverting input of A2 Op Amp goes low causing the output to go high.			Failure detector #1 will remain inoperative.
15	R15	Resistor	Current limits the inverter input current measurement to the A2 Op Amp.	Open		Non-inverting input of A2 Op Amp goes low causing the output to stay low.			Failure detector #1 can still sense voltage failures. Can't sense current failures.
16	R16	Resistor	Current limits the inverter output current measurement to A2 Op Amp.	Open		Inverting input of A2 Op Amp goes low causing the output to go high.			Failure detector #1 will remain inoperative.
17	R17	Resistor	Converts the AC current measurement to a voltage level.	Open		Voltage level goes high. A2 Op Amp output stays low.			Failure detector #1 can still sense voltage failures. Can't sense current failures.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
18	R18	Resistor	Converts the AC current measurement to a voltage level.	Open		Voltage level goes high. A2 Op Amp output stays low.			Failure detector #1 can still sense voltage failures. Can't sense current failures.
19	R19	Resistor	Feedback which determines the reset level of the current detector after having been tripped.	Open		No hysteresis. Op Amp output oscillation could occur if inverter currents were right at the trip point.			Failure detector #1 would not be effective for identifing small current failures.
20	R20	Resistor	Provides discharge path for time delay capacitor C7 (transient suppression delay)	Open		After detecting the first inverter failure, the capacitor would remain charged just below the zener voltage. There would be no time delay the next time A1 or A2 goes high.		Signals from two of the three failure detectors are required before any action is taken. The second failure detector would still have its time delay hence would delay the action.	
21	R21	Resistor	Limits the charge current into time delay capacitor C7.	Open		Loss of output to the majority vote circuit.			Failure detector #1 will remain inoperative.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
22	R22	Resistor	Limits base drive to Q1	Open		The combination of FD #1 & FD #2 in the voting circuit won't work.		Combination of FD #1 & #3 of FD #2 & #3 will provide proper operation.	
23	R23	Resistor	Limits base drive to Q2	Open		the combination of FD #1 & #3 in the voting circuit won't work.		Combination of FD #2 & #3 or FD #1 & #2 will provide proper operation.	
24	CR1	Diode	Provides isolation for the energy storage circuit in the event of an under-voltage condition on the protected Bus.	Open		Capacitor C3 can't be charged from the protected Bus		C3 can be charged from the Main Bus.	
				Short		NONE		CR 1 is backed up by series redundant CR2	

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
25	CR2	Diode	Provides isolation for the energy storage circuit in the event of an under-voltage condition on the protected Bus.	Open		Capacitor C3 can't be charged from the protected Bus.		C3 can be charged from the Main Bus.	
				Short		NONE		CR2 is backed up by series redundant CR1	
26	CR3	Diode	Provides isolation for the energy storage circuit in the event of an under-voltage on the Main Bus.	Open		Capacitor C3 can't be charged from the Main Bus.		C3 can be charged from the Protected Bus.	
				Short		NONE		CR3 is backed up by series redundant CR4	
27	CR4	Diode	Provides isolation for the energy storage circuit in the event of an under-voltage on the Main Bus.	Open		Capacitor C3 can't be charged from the Main Bus.		C3 can be charged from the Protected Bus.	
				Short		NONE		CR4 is backed up by series redundant CR3	

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
28	CR5	Diode	Rectifies the inverter AC output voltage to a DC signal	Open		None - The discharge time constant of C1 is so long that the half wave rectification will limit the C1 discharge to 0.6 volts.			
				Short		Puts a short circuit on the secondary of T1 every other half cycle. A-1 Op Amp output will stay high.		Current drawn from the T1 primary is limited by resistor R1.	Failure detector #1 will remain inoperative.
29	CR6	Diode	Rectifies the inverter AC output voltage to a DC signal	Open		None - The discharge time constant of C1 is so long that the half wave rectification will limit the C1 discharge to 0.6 volts.			
				Short		Puts a short circuit on the secondary of T1 every other half cycle. A-1 Op Amp output will stay high.		Current drawn from the T1 primary is limited by resistor R1.	Failure detector #1 will remain inoperative.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
30	CR7	Diode	Compensates for variation of voltage drop of CR5 and CR6 due to temperature changes.	Open		Inverting input to A-1 Op Amp goes high, causing output to remain low.			Failure detector #1 can still sense current failures. Can't sense voltage failures.
				Short		Inverting input to A-1 Op Amp goes low, causing the output to go high.			Failure detector #1 will remain inoperative.
31	CR8	Diode	Provides isolation so that a high output of A-2 Op Amp is not grounded by a low output of A-1 Op Amp.	Open		Loss of A-1 output			Failure detector #1 can still sense current failures. Can't sense voltage failures.
				Short		NONE		CR8 is backed up by series redundant CR9	
32	CR9	Diode	Provides isolation so that a high output of A-2 Op Amp is not grounded by a low output of A-1 Op Amp.	Open		Loss of A-1 output			Failure detector #1 can still sense current failures. Can't sense voltage failures.
				Short		NONE		CR9 is backed up by series redundant CR8	

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
33	CR10	Diode	Provides discharge path for energy storage capacitor C3 into the detector circuits.	Open		Failure detector 1 won't operate from the energy storage circuit as the series resistance of R9 is too large.			Failure detector #1 will still operate with either a good Main or Protected Bus.
				Short		The charging current to C3 would be limited by only the source RTG resistance. Current would fail the diodes CR1, 2, 3 and 4.			Failure detector #1 will be inoperative if diodes CR1 thru CR4 are failed.
34	CR11	Diode	Rectifies the AC reference voltage used in the inverter DC input current sensor circuit.	Open		Core of winding 3-4 of saturable reactor T4 would saturate. Output of DC current sensor to A-2 non-inverting input would go low, causing A-2 output to stay low.			Failure detector #1 can still sense voltage failures. Can't sense current failures.
				Short		During one half cycle, both cores of T4 will saturate. Saturation current will flow thru windings 1-2 & 3-4 back to the secondary of T2. No current transformation will take place between the two secondaries of T4. The non-inverting input to A-2 will go low.	Current transients will appear on the A.C. reference		Failure detector #1 can still sense voltage failures. Can't sense current failures.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
35	CR12	Diode	Rectifies the AC reference voltage used in the inverter DC input current sensor circuit.	Open		Core of winding 3-4 of saturable reactor T4 would saturate. Output of DC current sensor to A-2 non-inverting input would go low, causing A-2 output to stay low.			Failure detector #1 can still sense voltage failures. Can't sense current failures.
				Short		During one half cycle, both cores of T4 will saturate. Saturation current will flow thru windings 1-2 & 3-4 back to the secondary of T2. No current transformation will take place between the two secondaries of T4. The non-inverting input to A-2 will go low.	Current transients will appear on the AC reference.		Failure detector #1 can still sense voltage failures. Can't sense current failures.
36	CR13	Diode	Rectifies the inverter AC output current to a DC current signal.	Open		Voltage across R17 & R18 will drop. This lowers the inverting input to A-2 Op Amp, which causes the output to go high.			Failure detector #1 will remain inoperative.
				Short		Voltage across R17 & R18 will drop. This lowers the inverting input to A-2 Op Amp, which causes the output to go high.		Due to the number of turns in T3 secondary and also the turns ratio, the effective impedance of this short is very low.	Failure detector #1 will remain inoperative.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
37	CR14	Diode	Rectifies the inverter AC output current to a DC current signal.	Open		Voltage across R17 & R18 will drop. This lowers the inverting input to A-2 Op Amp, which causes the output to go high.			Failure detector #1 will remain inoperative.
				Short		Voltage across R17 & R18 will drop. This lowers the inverting input to A-2 Op Amp, which causes the output to go high.		Due to the number of turns in T3 secondary and also the turns ratio, the effective impedance of this short is very low.	Failure detector #1 will remain inoperative.
38	CR15	Zener Diode	Provides bias of the current measurement such that comparisons of input to output current ceases when currents get very low.	Open		Inverting input of A-2 Op Amp goes low causing output to go high.			Failure detector #1 will remain inoperative.
				Short		Inverting input of A-2 Op Amp goes high causing output to remain low.			Failure detector #1 can still sense voltage failure. Can't sense current failure.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
39	CR16	Diode	Provides isolation so that a high output of A-1 Op Amp is not grounded by a low output of A-2 Op Amp	Open		Loss of A-2 output.			Failure detector #1 can still sense voltage failures. Can't sense current failures.
				Short		NONE		CR16 is backed up by series redundant CR17	
40	CR17	Diode	Provides isolation so that a high output of A-1 Op Amp is not grounded by a low output of A-2 Op Amp	Open		Loss of A-2 output.			Failure detector #1 can still sense voltage failures. Can't sense current failures.
				Short		NONE		CR17 is backed up by series redundant CR16	
41	CR18	Diode	NONE	Open		NONE			Remove CR18 from circuit
				Short		Time delay of R21-C7 is lost. C7 changes instantaneously.	NONE	Signals from two of the three failure detectors are required before any action is taken. The second failure detector would still have its time delay hence would delay the action.	

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
42	CR19	Zener Diode	Minimum output of Op Amps A-1 & A-2 would not allow transistors Q1 & Q2 to fully cut-off. This zener provides the required voltage drop for cut-off.	Open		Loss of output from both Op Amps.			Failure detector #1 would remain inoperative.
				Short		Transistors Q1 & Q2 would not be completely cut-off.		The voting transistors above or below Q1 & Q2 are cut-off thus preventing inverter switching.	
43	CR20	Diode	Provides isolation of the majority voting circuit in the event of an undervoltage condition on the Protected Bus.	Open		Protected Bus can't keep the output of the majority voting circuit high when there is no inverter failure.		The Main Bus can keep the output high.	
				Short		NONE		CR20 is backed up by series redundant CR21	

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
44	CR21	Diode	Provides isolation of the majority voting circuit in the event of an under-voltage condition on the Protected Bus.	Open		Protected Bus can't keep the output of the majority voting circuit high when there is no inverter failure.		The Main Bus can keep the output high.	
				Short		NONE		CR21 is backed up by series redundant CR20.	
45	CR22	Diode	Provides isolation of the majority voting circuit in the event of an under-voltage condition on the Main Bus	Open		The Main Bus can't keep the output of the majority voting circuit high when there is no inverter failure.		The Protected Bus can keep the output high.	
				Short		NONE		CR22 is backed up by series redundant CR23	

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
46	CR23	Diode	Provides isolation of the majority voting circuit in the event of an under-voltage condition on the Main Bus.	Open		The Main Bus can't keep the output of the majority voting circuit high when there is no inverter failure.		The Protected Bus can keep the output high.	
				Short		NONE		CR23 is backed up by series redundant CR22.	
47	CR24	Diode	To protect the output level of the majority vote circuit in the event of a collector base short of transistor Q2.	Open		Loss of base drive to Q2		The other two combinations of failure detectors are operable.	Loss of the FD #1 & FD #3 combination in the majority voting circuit.
				Short		None unless Q2 fails short circuit collector to base.			
48	CR25	Diode	To protect the output level of the majority vote circuit in the event of a collector base short of transistor Q1.	Open		Loss of base drive to Q1		The other two combinations of failure detectors are operable.	Loss of the FD #1 & FD #3 combination in the majority voting circuit.
				Short		None unless Q1 fails short circuit collector to base.			

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
49	C1	Capacitor	Filters the rectified measurement of the inverter output voltage.	Open		None - Ratio of on to off time by AC input is 50:1 while ratio of charge to discharge time constant of C7 is 10:1. Therefore there is no build up of voltage on C7.			
				Short		Rectified AC voltage would be short circuited. Current from AC Bus is limited by R1. Inverting input to A-1 Op Amp goes low causing output to go high.			Failure detector #1 would remain inoperative.
50	C2	Capacitor	Frequency compensation for A-1 Op Amp.	Open		Op Amp will oscillate			Failure detector #1 would remain inoperative.
				Short		Op Amp output will go high.			Failure detector #1 would remain inoperative.
51	C3	Capacitor	Provide energy storage to operate FD#1 in the event that Main & Protected Bus voltages are low.	Open		FD #1 won't operate if both buses are low			
				Short		FD #1 won't operate if both buses are low.			9M-watts of power will be dissipated in R9.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
52	C4	Capacitor	Filters the output of the DC current sensor.	Open		Will cause the non-inverting input of A-2 Op Amp to go high causing the output to go high.			Failure detector #1 will remain inoperative.
				Short		Non-inverting input of A-2 Op Amp will go low causing output to remain low.			Failure detector #1 can still sense voltage failures. Can't sense current failures.
53	C5	Capacitor	Filters the output of the AC current sensor.	Open		None - Ratio of on to off time by AC input is 50:1 while ratio of charge to discharge time constant of C7 is 10:1. Therefore there is no build up of voltage on C7.			
				Short		Rectified current would be shorted. Inverting input to A-2 Op Amp would go low causing the output to go high.			Failure detector #1 would remain inoperative.
54	C6	Capacitor	Frequency compensation for A-2 Op Amp.	Open		Op Amp will oscillate			Failure detector #1 would remain inoperative.
				Short		Op Amp output will go high.			Failure detector #1 would remain inoperative.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
55	C7	Capacitor	Time delay to provide transient immunity.	Open		Q1 & Q2 will turn on immediately when one of the Op Ampsgoes high.		Signals from two of the three failure detectors are required before any action is taken. The second failure detector would still have its time delay hence would delay the action.	
56	T1	Transformer	Isolates the inverter output voltage detection circuitry from the AC bus.	Open		Loss of measurement of output voltage causes inverting input to A-2 Op Amp to go low and the output will then go high.			Failure detector #1 will remain inoperable.
				Short		Loss of measurement of output voltage causes inverting input to A-2 Op Amp to go low and the output will then go high. Short circuit current is limited by R1.			Failure detector #1 will remain inoperable.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
57	T2	Transformer	Provides an AC reference for the DC current sensor.	Open		Loss of inverter input current measurement. A-2 Op Amp non-inverting input goes low causing the output to stay low.			Failure detector #1 can still detect voltage failures. Can't detect current failures.
				Short		Loss of inverter input current measurement. A-2 Op Amp non-inverting input goes low causing the output to stay low.	Short on the primary winding 1-2 will short circuit the Protected Bus.		Add a fuse or current limiting resistor in series with the primary winding.
58	T3	Transformer	Allows sampling of the inverter AC output current.	Open or Short		Loss of inverter output current if the secondary windings fail. Inverting input of A-2 Op Amp goes low causing the output to go high.			Failure detector #1 will remain inoperable. The primary winding is a wire thru the center of the core. Don't consider it to fail open or short.
59	T4	Saturable Reactor	Magnetically amplify the inverter DC input current for the detection circuitry.	Winding open circuit or short circuit		Loss of current measurement will cause non-inverting input of A-2 Op Amp to go low which keeps the output low.			Failure detector #1 can still detect voltage failures. Can't detect current failures.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No.

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
60	A1	Operational Amplifier	Compares the inverter input voltage with the output voltage to determine out of spec. operation.	Output High		Keeps transistors Q1 and Q2 on.			Failure detector #1 will remain inoperable.
				Output Low		Failure Detector #1 would not respond to an out of spec. voltage condition.			Failure detector #1 can still detect current failures.
61	A2	Operational Amplifier	Compares the inverter input current with the output current to determine out of spec. operation.	Output High		Keeps transistors Q1 and Q2 on.			Failure detector #1 will remain inoperable.
				Output Low		Failure Detector #1 would not respond to an out of spec. current condition.			Failure detector #1 can still detect voltage failures.

Table 5.8-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component INVERTER FAILURE DETECTOR
Drawing No. _____

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
62	Q1	Transistor	In conjunction with a transistor from FD#2, it causes the output of the voting circuit to go low which causes a response in the inverter switch command generator.	Open		Loss of the FD #1 & FD #2 combination in the majority voting circuit.		The other two combinations of failures detectors are operable.	
				Short		The FD #1 & FD #2 combination in the majority voting circuit will be controlled by FD#2 only.			
63	Q2	Transistor	In conjunction with a transistor from FD#3, it causes the output of the voting circuit to go low which causes a response in the inverter switch command generator.	Open		Loss of theFD #1 & FD #3 combination in the majority voting circuit.		The other two combinations of failures detectors are operable.	
				Short		The FD #1 & FD #3 combination in the majority voting circuit will be controlled by FD#3 only.			

5.9 POWER DISTRIBUTION CIRCUITRY

The functional requirements for both the power distribution switches and load current limiters are provided in Section 4.3.4. These requirements were derived by analyzing the individual spacecraft loads to determine mission importance, level of redundancy, power level, effect of switch failure, etc., as shown on Table 4.3-1.

The following sections describe each component operation with reference to its schematic, the breadboard test results, and for those devices selected for use in the TOPS baseline design and documents, a Failure Mode, Effect, and Criticality Analysis.

5.9.1 RELAY SWITCH

5.9.1.1 Design Description (Figure 5.9-1)

This design uses two relays with contacts "Quaded" to achieve high reliability and single failure immunity. No single piece part failure will prevent subsequent turn on or turn off.

Transfer of either relay will make or break the load path. The logic to determine which coil of a relay is energized, for a particular command, is done by the contacts of the other relay. The commands from CCS are applied to both relay drivers, but to avoid oscillation or races the command is delayed to K2 relay driver until command to K1 drivers has been removed. This allows sufficient time for K1 to transfer. The delay is done by the Q7, Q8 circuit which latches on for the duration of the time constant of 160 KΩ and 0.22 uf (C5) in the base drive of Q8. While the command (OFF 1) is still present, Q7 is in saturation and prevents the Q8 collector current from reaching Q9, thus delaying the command to Q9.

Capacitors C1-C4 prevent the effect of a continuous command if a transistor fails short in the circuitry leading up to that point. An alternative approach, particularly applicable to K1 driver, is to make Q3 (and Q6) two transistors, one each for Q1 and Q2 (Q4 and Q5). This would also prevent a single part failure from applying continuous signal to both PNP coil drivers.

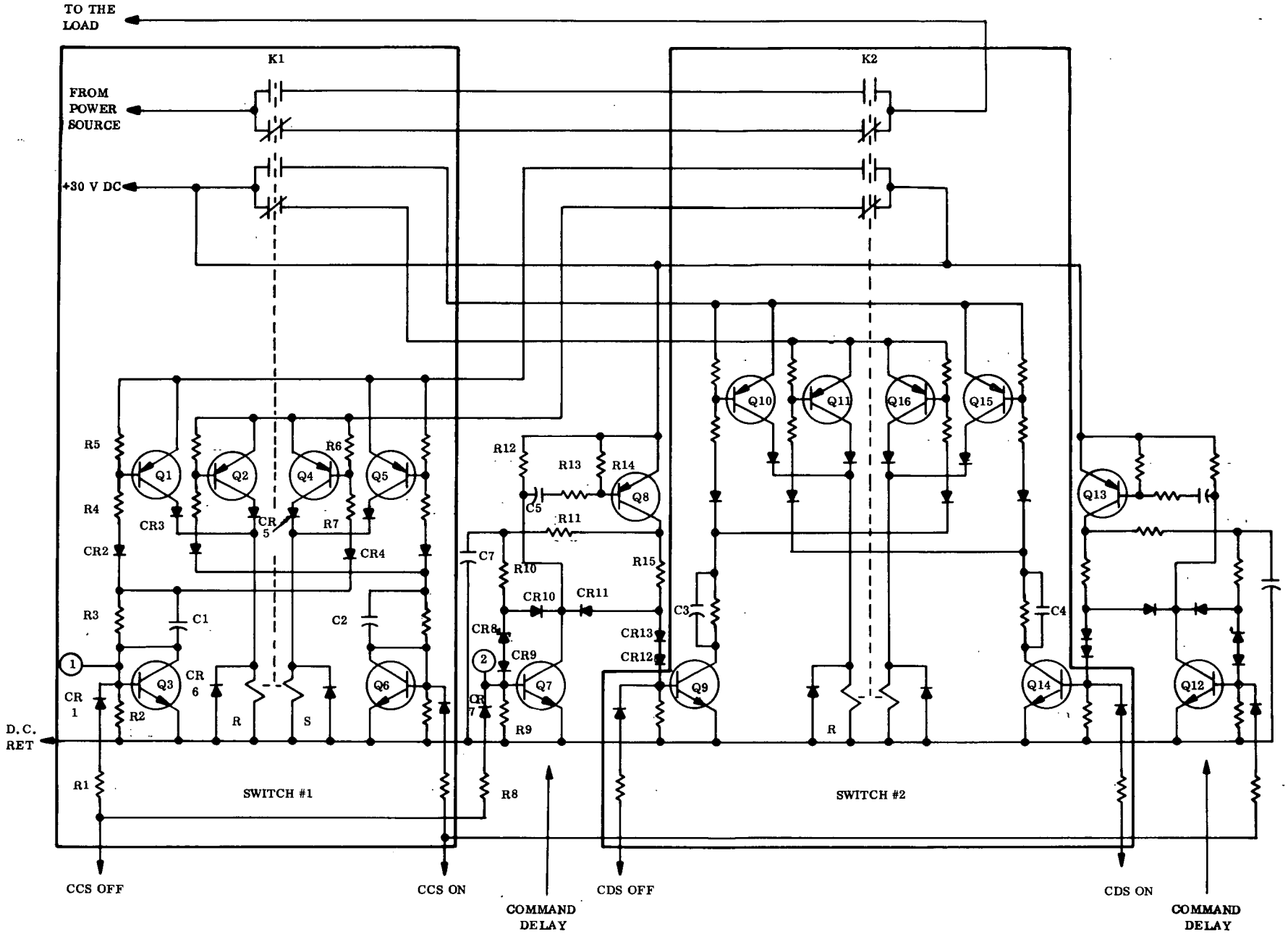


Figure 5.9-1. Relay Switch Schematic

Since the K2 circuit contains some high impedance circuits (Q7, Q8 and Q12, Q13) some trouble with noise sensitivity was encountered associated with the transients at turn-on and turn-off. The 3300 pf capacitors in the base drive to Q7 and Q12 provides several milliseconds delay in the self latching of the Q7, Q8 and Q12, Q13 circuits, which completely eliminates erroneous responses due to transients. The diode input for all command sources provides isolation for other command sources and some noise immunity. The diode was used to maintain commonality even where there were no second command sources.

5.9.1.2 Test Results

The equipment used to test the switch performance was configured as shown on Figure 5.9-2. A command generator was custom built using SN5400 TTL gate outputs. All ac voltages were measured by a Fluke rms ac voltmeter. Load current was determined by dividing the measured output voltage by the measured load resistance. DC power consumption was determined by multiplying the measured input voltage by the reading of a current meter in the dc supply lines.

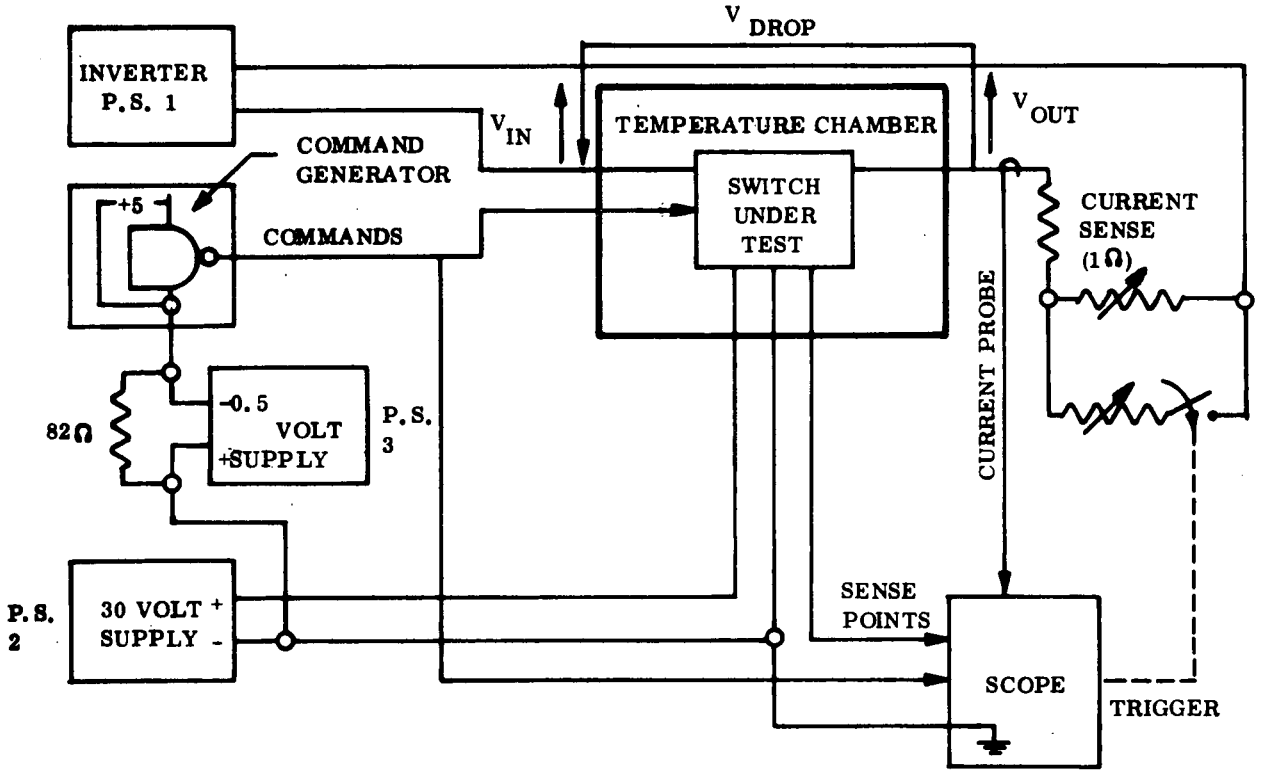


Figure 5.9-2. Switch Evaluation Test Set Up

Minimum command voltage was determined by slowly raising the command voltage until the command input under test responded normally. The command voltage was varied by biasing the command generator negative with respect to the switch command return. The biasing was done by PS 3 in Figure 5.9-2. The command voltage was measured by the deflection above ground on an oscilliscore trace of the command.

The relay switch breadboard unit is shown schematically in Figure 5.9-3. Tests were performed to determine the magnitude of the command signal required for switch response, and the minimum setting on the 30 volt supply at which the switch would operate. Both measurements were made over the temperature range of -25 to $+85^{o}$C. These results are plotted in Figure 5.9-4.

The qual relay switch of Figure 5.9-1 is primarily the same design except coupling capacitors were added in the collector of the command receiver transistor to prevent serious single failure modes. Figure 5.9-5 presents similar data as Figure 5.9-4 except for the unit relay switch.

The CCS commands require a higher voltage to obtain proper switch response to prevent a race or oscillation of the delay coupler to relay K2. The minimum bus voltage is also higher than the breadboard unit because of the interactions of the delay coupler.

The capacitive coupling of the command provides greater than 12 millisecond drive to K1 relay (time at which the voltage on the coil is greater than 90% of steady state maximum).

The delay coupler and capacitive coupling in the K2 driver provided a minimum 22 millisecond drive to the coil of K2. Figure 5.9-6 is a reproduction of the photograph of the on and off command and dc current waveforms for -20^{o}C where these minimums occurred.

The basic concept in the relay switch design is that no reasonable single piece part failure will cause irrevocable turn on or turn off. The resultant quaded contact design produces about the highest reliability design. All the preceding is based on the assumption that the probability of the relay falling completely apart is so remote as to be considered zero.

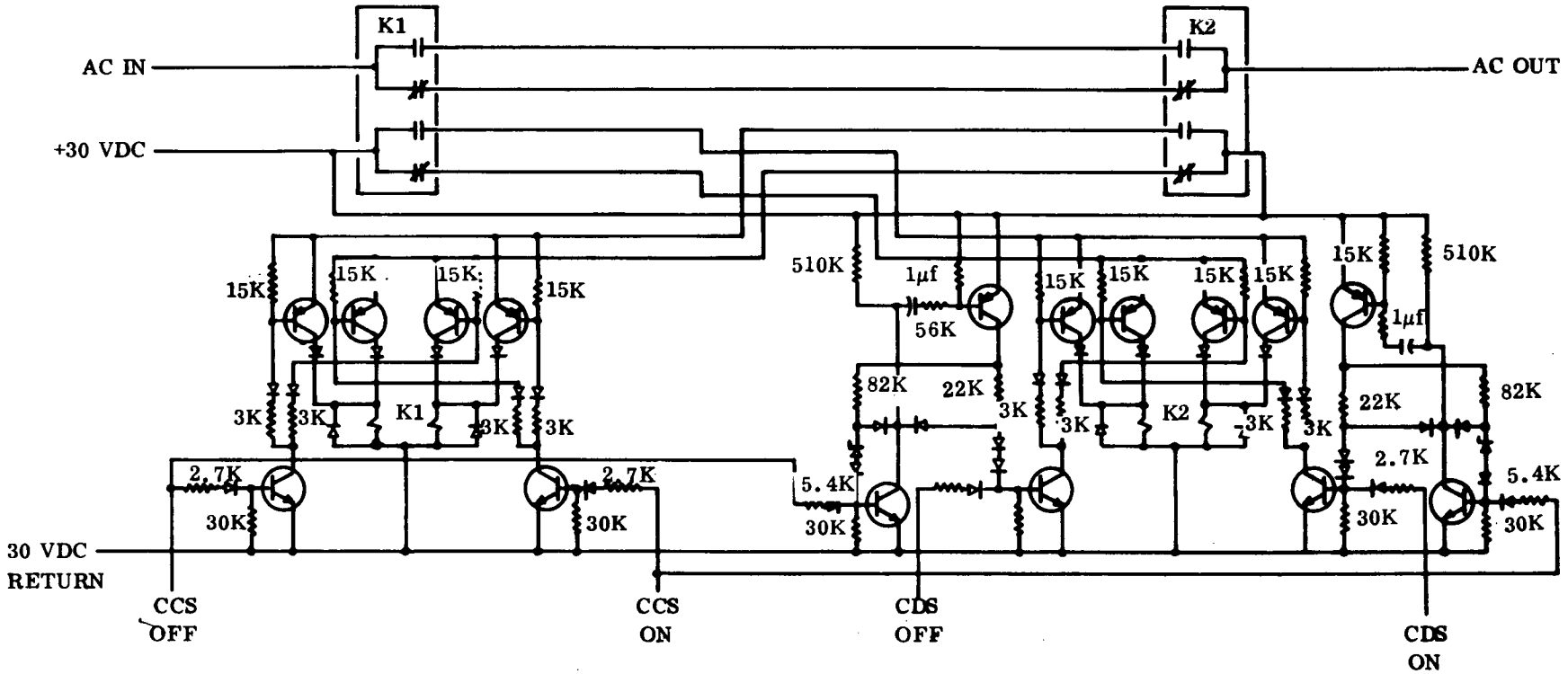


Figure 5.9-3. Relay Switch Breadboard Schematic

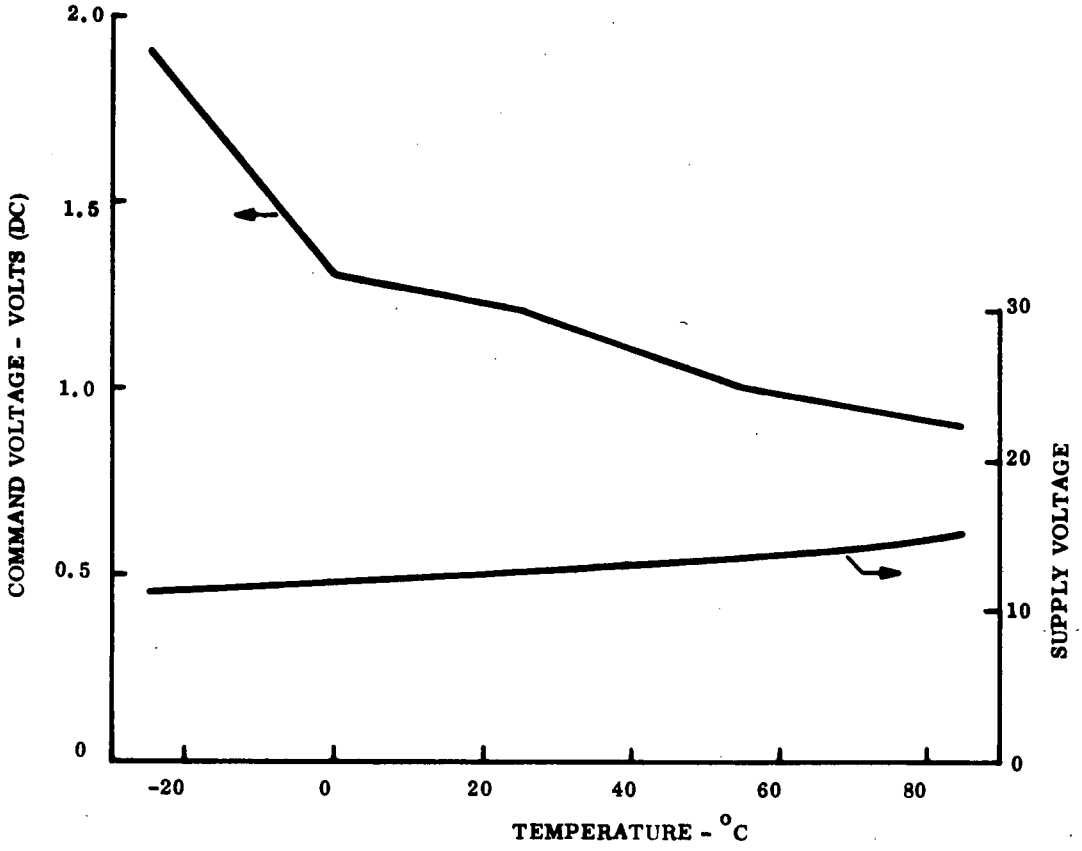


Figure 5.9-4. Relay Switch Breadboard Minimum Operational Voltages

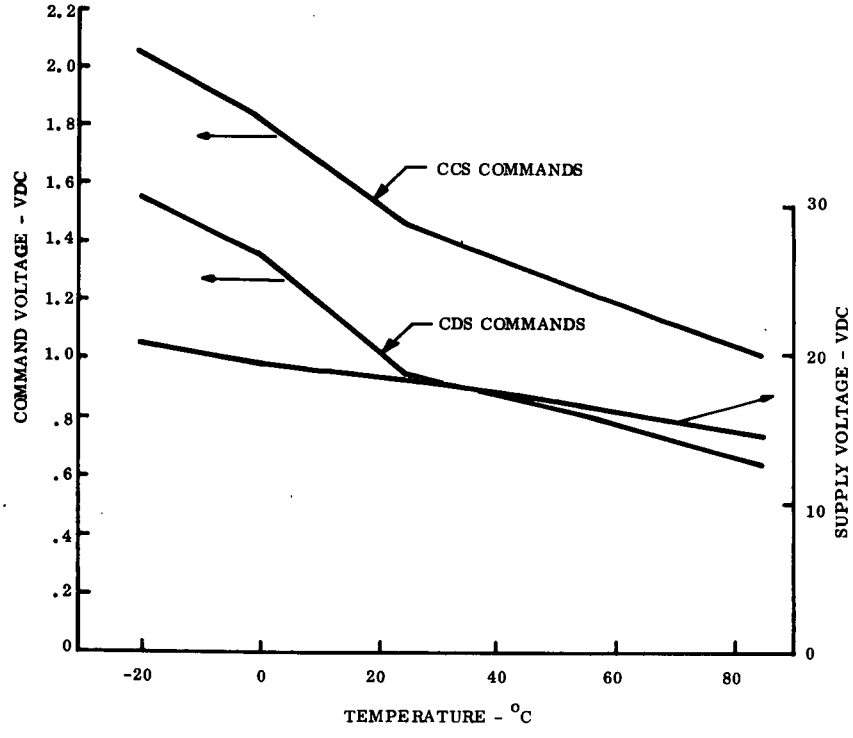


Figure 5.9-5. Relay Switch Qual Unit Minimum Operational Voltages for 100% Operation

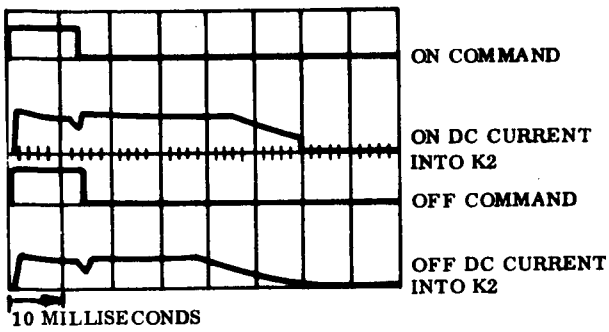


Figure 5.9-6. Relay Switch Qual Unit Coil Drive Pulse Width

The basic design is applicable to any relay coil resistance by merely changing component values. The design of Figure 5.9-1 is for a nominal 1500 Ω coil which covers 1/2 crystal can relays. This relay contact rating should suffice for all but a few loads on TOPS. Size and weight can be saved by using TO-5 type relays for the smaller loads.

5.9.1.3 Relay Switch Reliability

A study was performed to determine the effect on switch reliability if the assumption that there will be no catastrophic relay failures is incorrect. The following equation was used to find overall switch reliability (R_{sw}).

$$R_{sw} = R_{K1}\,[(1 - R_{K2}) \times \%\ \text{noncatastrophic}] + R_{K2}\,[(1 - R_{K1}) \times \%\ \text{noncatastrophic}] + R_{K1}\,R_{K2}$$

Where:

R_{K1} = Reliability of relay K1 and its associated circuitry

R_{K2} = Reliability of relay K2 and its associated circuitry

% noncatastrophic = all failures except those relay failures which completely open or close the power path through the switch.

These factors are determined as follows:

$$R_{K1} = e^{-\lambda_1 t}$$

$$R_{K2} = e^{-\lambda_2 t}$$

$$\%\ \text{noncatastrophic} = 1 - \frac{(\%\ \text{relay catastrophic}) \times \lambda R}{\lambda_1}$$

Where:

λ_1 = summation of all failure rates of K1 circuitry

$\lambda_1 = 2.274 \times 10^{-6}$

λ_2 = summation of all failure rates of K2 circuitry

$\lambda_2 = 2.560 \times 10^{-6}$

λ_R = relay failure rate

$\lambda_R = 2.0 \times 10^{-6}$

t = mission time

$t = 10^5$ hours

R_{sw} was then determined for three values of percent catastrophic relay failures. The results shown in Table 5.9-1 indicate that allowing for a small percent of catastrophic failures does not significantly change the relay switch reliability.

Table 5.9-1. Relay Switch Reliability

% Relay Catastrophic Failures	Relay Switch Reliability (R_{sw})
0	0.95406
0.5	0.95337
1.0	0.95127

5.9.1.4 Failure Mode, Effect, and Criticality Analysis - Relay Switch

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.9-2. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	R1	Resistor	Limit input current to Q3 from command source.	Open		Loss of SW #1 off capability.		SW #2 can turn off the power distribution switch	
2	R2	Resistor	Q3 leakage resistor.	Open		Q3 could turn on if leakage current was high.	If the power distribution switch was on, it would turn off.	The off signal is AC coupled by C1 so that the failure is nonrepetitive	Switch #1 can still turn on the power distribution switch. Turn off must be done by switch #2 which, because of the command delay, will take longer to get the load off.
3	R3	Resistor	Discharge path for C1.	Open		Loss of SW #1 off capability as the command is AC coupled.		SW #2 can turn off the power distribution switch	
4	R4	Resistor	Limits base current of Q1	Open		Q1 would be inoperative. SW#1 would not respond to an off command if SW #2 had previously changed state as a result of a CDS command.		SW #2 can turn off the power distribution switch.	
5	R5	Resistor	Q1 leakage resistor	Open		Q1 could turn on if leakage current was high.	If the power distribution switch was on, it would turn off.	The off signal is AC coupled by C1 so that the failure is nonrepetitive.	Switch #1 can still turn on The power distribution switch. Turn off must be done by switch #2 which, because of the command delay, will take longer to get the load off.

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
6	R6	Resistor	Q4 leakage resistor	Open		Q4 could turn on if leakage current was high.	If the power distribution switch was on it would turn off.	The off signal is AC coupled by C1 so that the failure is nonrepetitive.	Switch #1 can still turn on the power distribution switch. Turn off must be done by switch #2 which, because of the command delay will take longer to get the load off.
7	R7	Resistor	Limits base current of Q4	Open		Loss of SW #1 off capability.		SW #2 can turn off the power distribution switch	
8	R8	Resistor	Limits input current to Q7 from command source	Open		Loss of SW #2 off capability by CCS command.		SW #2 off can be operated by a CDS command.	SW #1 off can be operated by CCS command.
9	R9	Resistor	Q7 leakage	Open		Q7 could turn on if leakage current was high.	If the power distribution switch was on, it would turn off.	The off command to SW #2 would persist until C5 charged.	SW #2 could no longer be commanded off by the CCS command. Can be operated by CDS command. SW#1 still has capability to turn off.
10	R10	Resistor	Limits the current thru CR8 and base of Q7.	Open		Latch-up capability of command delay circuit is lost. When CCS command stops, Q7 will not stay on and results in loss of SW #2 off capability by CCS command.		SW #2 off can be operated by a CDS command.	SW #1 off can be operated by CCS command.

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
11	R11	Resistor	Limits the charge rate of C7	Open		Latch-up capability of command delay circuit is lost. When CCS command stops, Q7 will not stay on and results in loss of SW #2 off capability by CCS command.		SW #2 off can be operated by a CDS command.	SW #1 off can be operated by CCS command.
12	R12	Resistor	Discharge path for C5	Open		Loss of SW #2 off capability by CCS command.		SW #2 off can be operated by a CDS command.	SW #1 off can be operated by CCS command.
13	R13	Resistor	Controls rate of charge of C5. This determines the duration of the delayed CCS command to SW #2.	Open		Loss of SW #2 off capability by CCS command.		SW #2 off can be operated by a CDS command.	SW #1 off can be operated by CCS command.
14	R14	Resistor	Q8 leakage resistor	Open		Q8 could turn on if leakage current was high. SW #2 off command capability would be lost.	If the power distribution switch was on, it would turn off.	The off signal is AC coupled by C3 so that the failure is nonrepetitive.	SW #2 can still turn on the power distribution switch. Turn off can only be accomplished by SW #1.
15	R15	Resistor	Limits base drive to Q9	Open		Loss of SW #2 off capability.		SW #1 can turn off the power distribution switch	

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
16	CR1	Diode	Provides isolation for LVCO command (point 1) in the event of a low CCS command source.	Open		Loss of SW #1 off capability.		SW #2 can turn off the power distribution switch	
				Short		None unless the CCS command source fails low or Q3 shorts base to collector.			
17	CR2	Diode	Prevents loss of SW #2 position logic thru path R6-R7-R4-R5 due to short of Base-Collector transistor.	Open		Q1 would be inoperative. SW #1 would not respond to an off command if SW #2 had previously changed state as a result of a CDS command.		SW #2 can turn off the power distribution switch	
				Short		SW #2 position logic would be destroyed such that both coils of SW #1 relay would be energized by either an on or off command.		SW #2 will perform the proper switching function.	
18	CR3	Diode	Prevents reverse voltage on Q1 when Q2 turns on.	Open		Q1 won't activate the reset coil of SW #1. SW #1 won't respond to an off command if SW #2 had previously changed state as a result of a CDS command.		SW #2 can turn off the power distribution switch.	

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No. _____

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
18				Short		Magnitude of reverse voltage would fail Q1. SW #1 would not respond to an off command if SW #2 had previously changed state as a result of a CDS command.		SW #2 can turn off the power distribution switch.	
19	CR4	Diode	Prevents loss of SW #2 position logic thru path R6-R7-R4-R5.	Open		Q4 would be inoperative. SW #1 would not respond to an off command if SW #2 had previously changed state as a result of a CDS command		SW #2 can turn off the power distribution switch	
				Short		SW #2 position logic would be destroyed such that both coils of SW #1 relay would be energized by either an on or off command.		SW #2 will perform the proper switching function	
20	CR5	Diode	Prevents reverse voltage on Q4 when Q5 turns on.	Open		Q4 won't activate the set coil of SW #1. SW#1 won't respond to an off command.		SW #2 can turn off the power distribution switch	
				Short		Magnitude of reverse voltage would fail Q4. SW #1 won't respond to an off command.			

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
21	CR6	Diode	Relay coil transient suppression	Open		High current spikes would be generated thru Q1 or Q2 as they are cutting off. Could cause failure of Q1 or Q2.		SW #2 can turn off the power distribution switch	
				Short		Q1 or Q2 would turn on into a short circuit. Transistor will fail.			
22	CR7	Diode	Provides isolation for collector Base short of Q7.	Open		Loss of SW #2 off capability by CCS command.		SW #1 can turn off by CCS command. SW #2 can turn off by CDS command.	
				Short		None			
23	CR8	Zener Diode	After removal of CCS command from base of Q7, this zener causes VCE of Q7 to increase such that base drive is supplied to Q9	Open		The command delay circuit doesn't latch up, thus SW #2 won't respond to the CCS off comand.		SW #1 can turn off by CCS command. SW #2 can turn off by CDS command.	

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No. _____

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
23				Short		Q7 VCE won't be large enough to cause turn on of Q9, SW #2 won't respond to the CCS off command.			
24	CR9	Diode	Provides isolation to insure that the CCS command to Q7 doesn't find a sneak path to Q9.	Open		The command delay circuit doesn't latch up, thus SW #2 won't respond to the CCS off command.		SW #1 can turn off by CCS command. SW #2 can turn off by CDS command.	
				Short		Could prematurely activate SW #2 if Q7 base to emitter fails open.			
25	CR10	Diode	Clamps Q7 collector voltage after CCS command is removed. This reverse biases CR11 and allows Q9 to turn on.	Open		The command delay circuit doesn't latch up, thus SW #2 won't respond to the CCS off command.		SW #1 can turn off by CCS command. SW #2 can turn off by CDS command.	
				Short		Q7 would be turned on by the base current of Q8 via path R13, C5, CR8, CR9 to base of Q7.	If the power distribution switch was on, it would turn off.	The duration of the off command from the command delay circuit is limited by C5. As a result of this failure C5 will never discharge so the failure is nonrepetitive.	SW #2 could no longer be commanded off by the CCS command. Can be operated by CDS command. SW #1 still has capability to turn off.

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No. _____

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
26	CR11	Diode	Prohibits the output of Q8 from turning on Q9 until removal of CCS command.	Open		SW #2 is activated at the same time as SW #1. The switch position logic becomes scrambled as both switches are changing position. This continues for the duration of the command signal. The final position of the power distribution switch would be off.		The CDS command can positively turn off the power distribution switch.	
				Short		Q8 base current into flow thru Q9 switch will shut off.		SW #1 would be the only means of turning off the power distribution switch.	
27	CR12 CR13	Diode	Provide sufficient voltage drop to base of Q9 such that anode voltage of CR11 won't be high enough to turn Q9 on when Q7 is being driven by CCS command	Open		Loss of Q9 base drive from the command delay circuit. SW #2 won't turn off.		SW #1 can turn off by CCS command. SW #2 can turn off by CDS command.	
				Short		If Q7 VCE is not lower than the Q9 VBE turn on level		The CDS command can positively	

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
27						for the duration of the CCS command, Q9 could turn on. The result is the same as CR11 failing open (see item 26)		turn off the power distribution switch	
28	C1	Capacitor	Limits the duration of relay coil activation in the event of a failure of the CCS command high or Q3 short.	Open		Loss of SW #1 off capability.		SW #2 can turn off the power distribution switch	
				Short		None unless those failures in function column occur.			
29	C5	Capacitor	Determines the duration of the output command from the command delay circuit.	Open		Command delay circuit is inoperative. Can't turn off SW #2 with the CCS command.		SW #1 can turn off by CCS command. SW #2 can turn off by CDS command.	
				Short		Output of command delay circuit remains high. Q9 remains on.		Duration of SW #2 relay coil activation is limited by C3	SW #2 no longer responds to an off command.
30	C7	Capacitor	Provides the energy to keep Q7 on during the transition between drop out of CCS command and latch-up by Q8.	Open		Q7 shuts off after drop out of CCS command. SW #2 doesn't respond to the CCS off command		SW #1 can turn off by CCS command. SW #2 can turn off by CDS command	

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No. _____

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
30				Short		Latch up diodes are shorted. SW #2 doesn't respond to the CCS off command			
31	Q1	Transistor	Drives the reset coil of SW #1 to turn off the power distribution switch	Open		SW #1 would not respond to an off command if SW #2 had previously changed state as a result of a CDS command.		SW #2 can turn off the power distribution switch.	
				Short		If SW #2 changes state as a result of a CDS command, continuous power will be applied to the reset coil of SW #1. If the power distribution switch had been on, it will turn off.		SW #2 can turn on the power distribution switch	
32	Q3	Transistor	Amplifies the CCS off command to SW #1.	Open		SW #1 won't respond to the off comand.		SW #2 can turn off the power distribution switch.	
				Short		SW #1 will turn off the power distribution switch.		The capacitor C1 prevents this failure effect from repeating when SW #2 turns the power distribution switch back on.	

Table 5.9-2. Failure Mode, Effect, and Criticality Analysis (Cont)

Subsystem POWER
Component POWER DISTRIBUTION SWITCH
Drawing No. ____

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
33	Q4	Transistor	Drives the set coil of SW #1 to turn off the power distribution switch	Open		SW #1 would not respond to an off command if SW #2 had previously changed state as a result of a CDS command.		SW #2 can turn off the power distribution switch.	
				Short		If SW #2 changes state as a result of a CDS command, continuous power will be applied to the set coil of SW #1. If the power distribution switch had been on, it will turn off.		SW #2 can turn on the power distribution switch.	
34	Q7	Transistor	Supplies required bias for the off command to SW #2 after removal of CCS off command.	Open or Short		Command delay circuit doesn't latch-up. SW #2 won't respond to the CCS off command		SW #2 can turn off by CDS command. SW #1 can turn off by CCS command.	
35	Q8	Transistor	Provides the base drive to Q9 when Q7 supplies the required bias to CR11	Open		Command delay circuit doesn't latch-up. SW #2 won't respond to the CCS off command		SW #2 can turn off by CDS command. SW #1 can turn off by CCS command.	
				Short		Q9 remains on. If power distribution switch was on, it would turn off. SW #2 won't respond to any future off commands.		Output of Q9 is coupled by capacitor C3. Failure effect is nonrepetitive. SW #1 can turn off the power distribution switch.	

5.9.2 MAGNETIC SWITCH

5.9.2.1 Design Description (Figure 5.9-7)

The power control element of the magnetic switch is two saturable reactors which are biased into saturation by a common control winding. The ampere turns in the control winding must exceed the ampere turns due to load current to keep the saturable reactors saturated. This control current represents a loss and must be minimized. A control to reactor turns ratio of 20:1 was selected for test (~3% loss for 50 volt load).

While a single coil reactor can perform the on/off function, the control winding voltage when the switch was off would be ±1000 volts, which would be difficult to handle. The two reactor circuit tends to produce spikes in the control winding which must be eliminated by several shorted turns around both saturable reactors, or by providing the approximate equivalent by a "low" impedance across the control winding, which was the method used.

The current in the control winding is switched by a quad transistor current switch. The quad current switch is controlled by a quad driver/command receiver circuit which provides high reliability and single failure protection in the command and control circuit. Since the magnetics contain no single failure modes which short the ac bus, no special protection or back-up is needed in that part of the circuit.

5.9.2.2 Test Results

The configuration of test equipment was identical to that of the relay switch described in Section 5.9.1.2.

Figure 5.9-8 shows the effect on series voltage losses for variations of load and temperature. Half the voltage loss for the curves of $R_L = 250$ and 275 ohms is attributed to the series resistance of the mag-amp windings. This resistance of approximately 1.4 ohms causes about 0.3 volts drop.

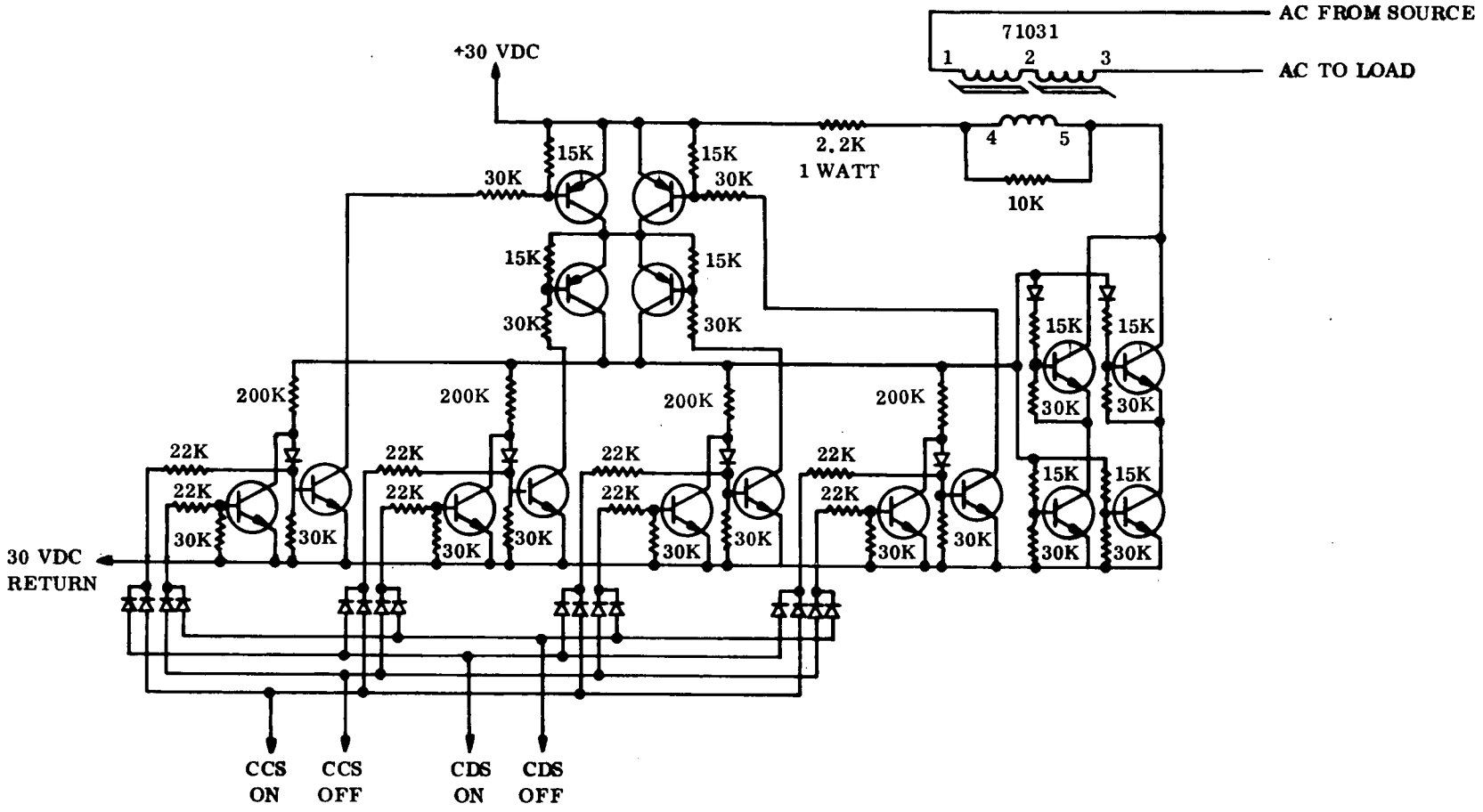


Figure 5.9-7. Magnetic Switch Schematic

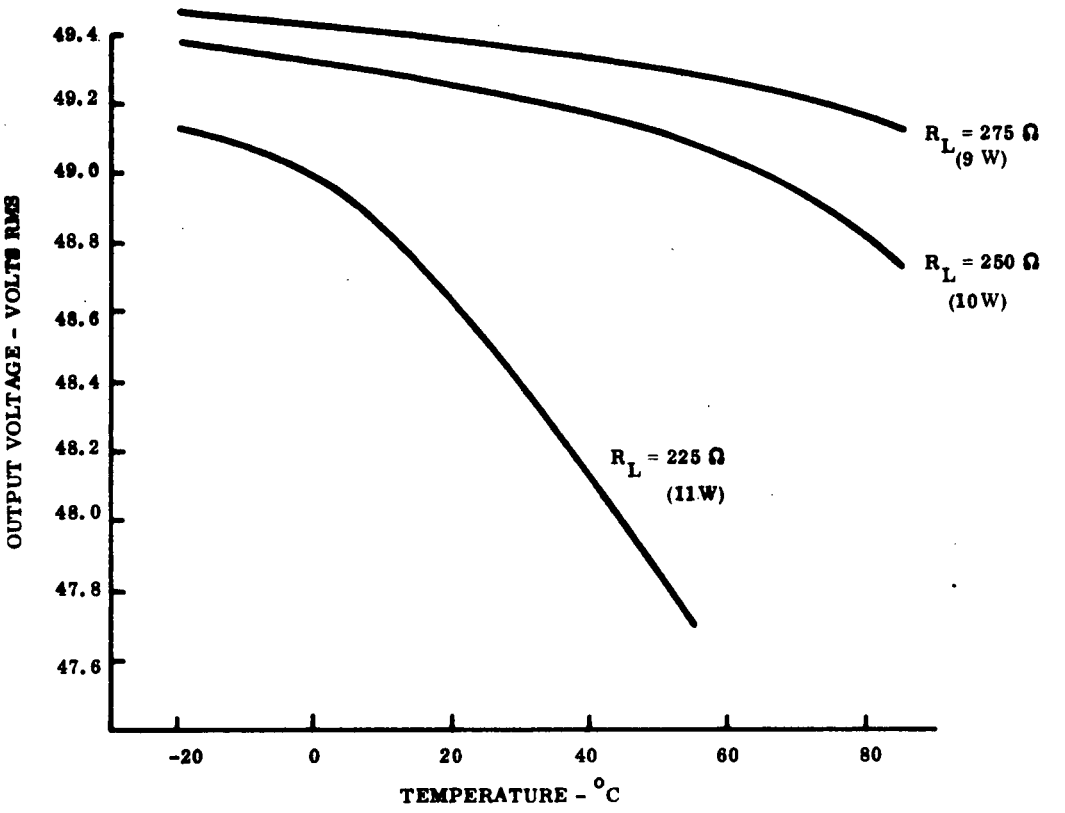


Figure 5.9-8. Magnetic Switch (10 Watt) Output Voltage

The rest of the voltage drop is due to inductive effects since there are large voltage spikes during commutation. The resistive effect is evident in the increase of drop with temperature. It is important to note the rapid increase in voltage loss at 225 Ω load. This is due to the saturable reactors becoming unsaturated. The 225 Ω curve shows that the magnetic switch should not be operated too close to the control current limit to avoid undervoltage at turn on or due to unknowns in load power consumption. The change versus temperature and load represents a loss in regulation which must be considered in specifying user load input voltage. These variations can be somewhat reduced at the expense of weight by decreasing turns and increasing wire size.

Figure 5.9-9 shows the ac power consumed when the switch is OFF and the dc control power when the switch is ON.

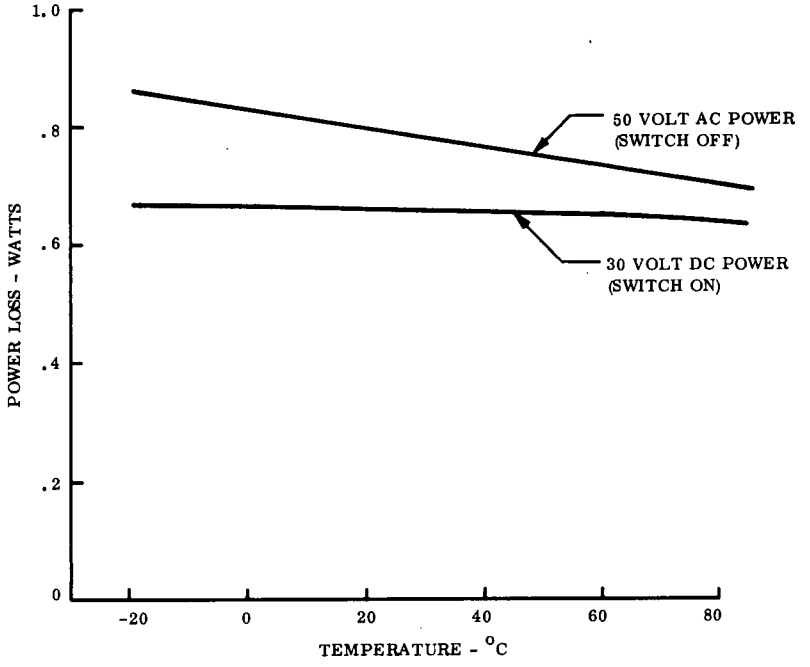


Figure 5.9-9. Magnetic Switch Schematic Off AC Power Consumption and On DC Power Consumption

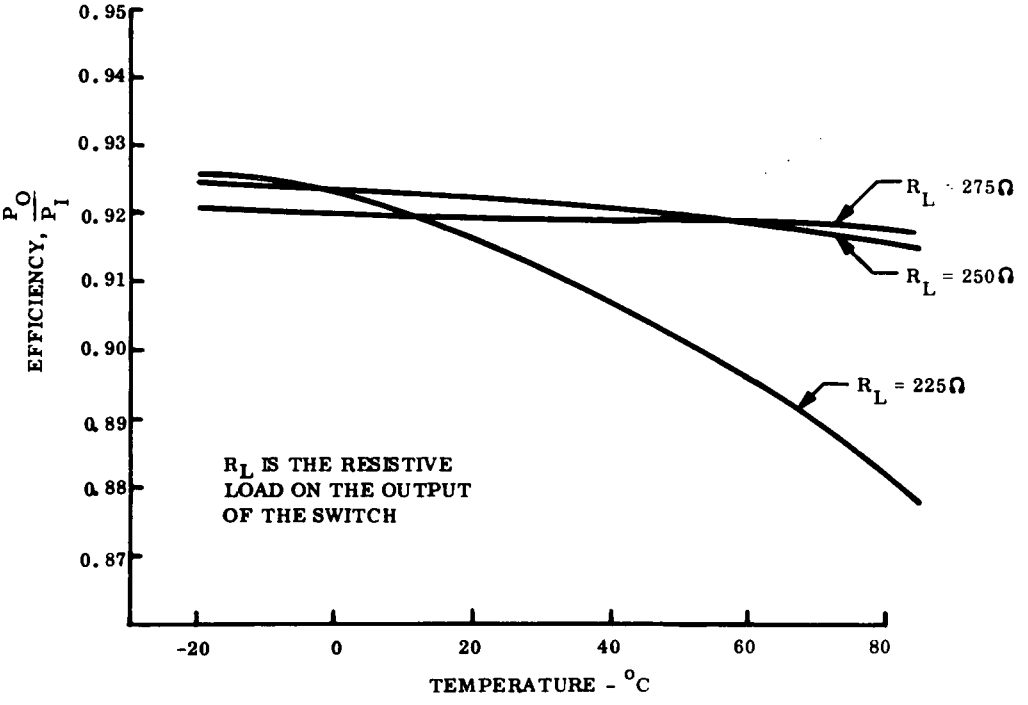


Figure 5.9-10. Magnetic Switch (10 Watt) Efficiency as a Function of Temperature

When OFF, the switch magnetization current becomes a power load on the ac greater than 800 milliwatts for this design. Magnetization current can be reduced by adding turns or using different material such as Permalloy 80, but both of these would result in increased weight and a tendency to increase series resistance. When ON, the switch consumes 30 volt dc power for the control current and command electronics. This power could be reduced by driving the control winding and electronics from a lower voltage, but that power supply is then a series item to all power switching and is an additional size and weight penalty.

Figure 5.9-10 summarizes all the switch losses in the form of efficiency. Efficiency was determined by dividing the power out to the load by the total ac and dc power into switch. A slight overload ($R_L = 225\,\Omega$) drastically reduces efficiency as temperature increases. Also, since the dc losses are relatively constant, underloading ($R_L = 275\,\Omega$) results in a low efficiency. Operation at approximately 10 percent below control current design ($R_L = 275\,\Omega$) is probably near optimum for efficiency and regulation.

Figure 5.9-11 shows the minimum command voltages required for switch response. Figure 5.9-12 presents the dc control voltage at which the switch turns off without command. It must be remembered that turn off will occur if the dc supply bus drops below this curve for only a short time (< 1 millisecond) and will remain off despite bus voltage recovery to normal.

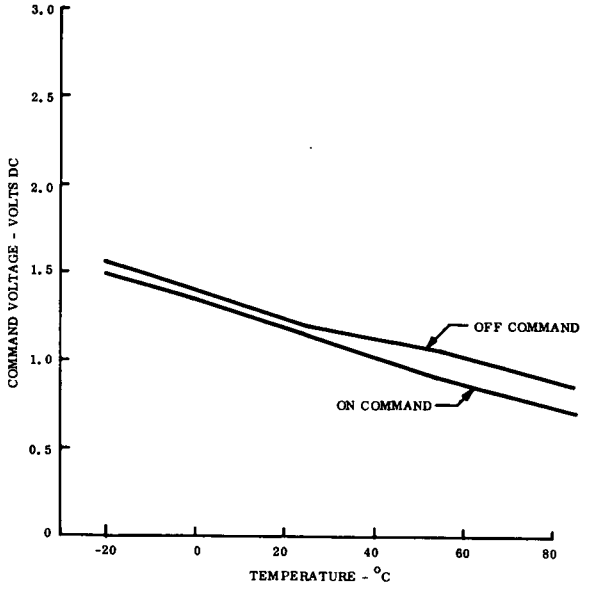


Figure 5.9-11. Magnetic Switch Minimum Command Voltage

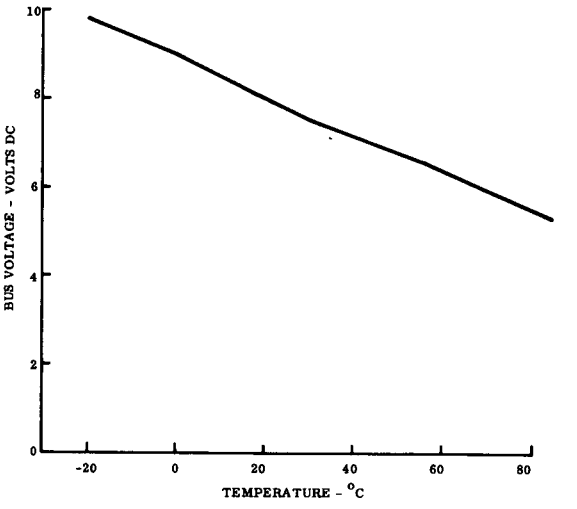


Figure 5.9-12. Magnetic Switch Dropout Voltage

Pictures of turn on and turn off were taken to determine these characteristics. The switch was fully on within 4 milliseconds from the start of the ON command and off within 2 milliseconds from the start of the OFF command.

This switch primarily has single failure modes in the coils and control resistor which prevent load turn on. It seems too high a weight and efficiency penalty to double the magnetics to prevent single failure turn off. The "off" power and the "on" efficiency can only be improved with weight and size increase. The current limiting advantage of the saturable reactor switch is practically lost because the current magnitude rapidly increases as the load resistance is decreased. This is due to the high turns ratio, which must be maintained for efficiency, and because there is no feedback from the output to cause cutoff for low load resistances. The efficiency and regulation degradation are severe compared to the relay switch, but good compared to the transistor switch of Section 5.9.3.

5.9.2.3 Magnetic Switch Reliability

Reliability of this switch design was determined from the reliability diagram of Figure 5.9-13.

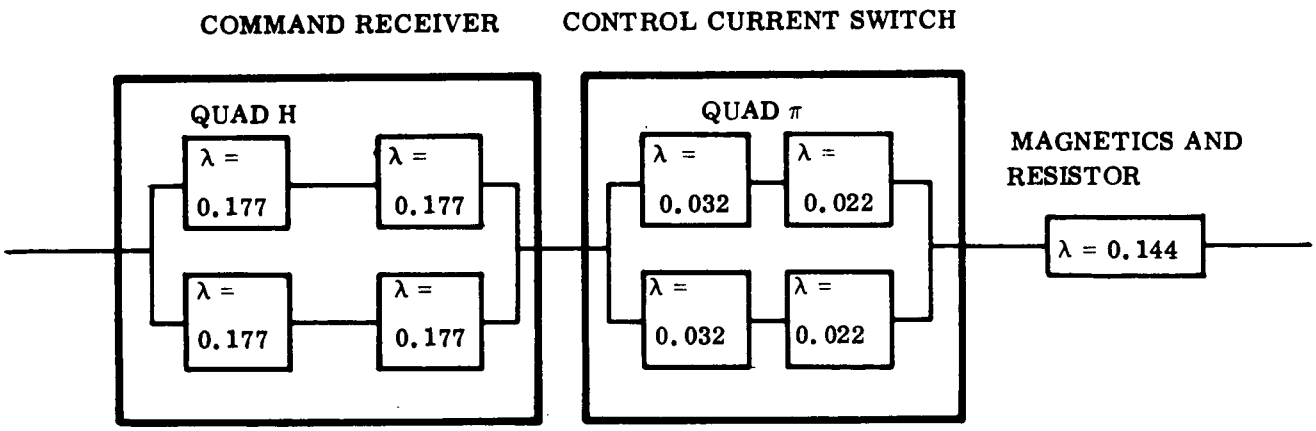


Figure 5.9-13. Magnetic Switch Reliability Model

The summation of piece part failure rates for each circuit is shown within the blocks. It was assumed that the probability of failures open equals the probability of failures short. Therefore, the equation for the quad H and quad π is the same and reduces to:

$$R_{quad} = 1 - \frac{Q_i^2}{2} [3 - Q_i]$$

where $Q_i = 1 - R_i$

R_i = reliability of one element of the quad

$R_i = e^{-\lambda_i t}$

The total switch reliability is found from the product of the reliabilities of the command receiver, the control current switch, and the magnetics. The results are shown in Table 5.9-3 for a mission time of 10^5 hours.

Table 5.9-3. Total Switch Reliability

Command Receiver Reliability	Control Current Switch Reliability	Magnetics Reliability	Total Magnetic Switch Reliability
0.999596	0.999985	0.9857	0.9853

5.9.3 AC SOLID STATE SWITCH

5.9.3.1 Design Description (Figure 5.9-14)

An ac solid state switch or transistor switch as it will be referred to is similar to the magnetic switch except the magnetic amplifier has been replaced with a diode bridge. The ac load current is rectified to dc and then controlled by the transistor switches.

The diode bridge must contain two diodes in series at each location to prevent half wave voltage to the load if a diode failed short when the switch is off. This would be a half wave short circuit since the load transformer would saturate under the equivalent of dc voltage applied to the primary. A quad was used at each location on the bridge to maximize reliability.

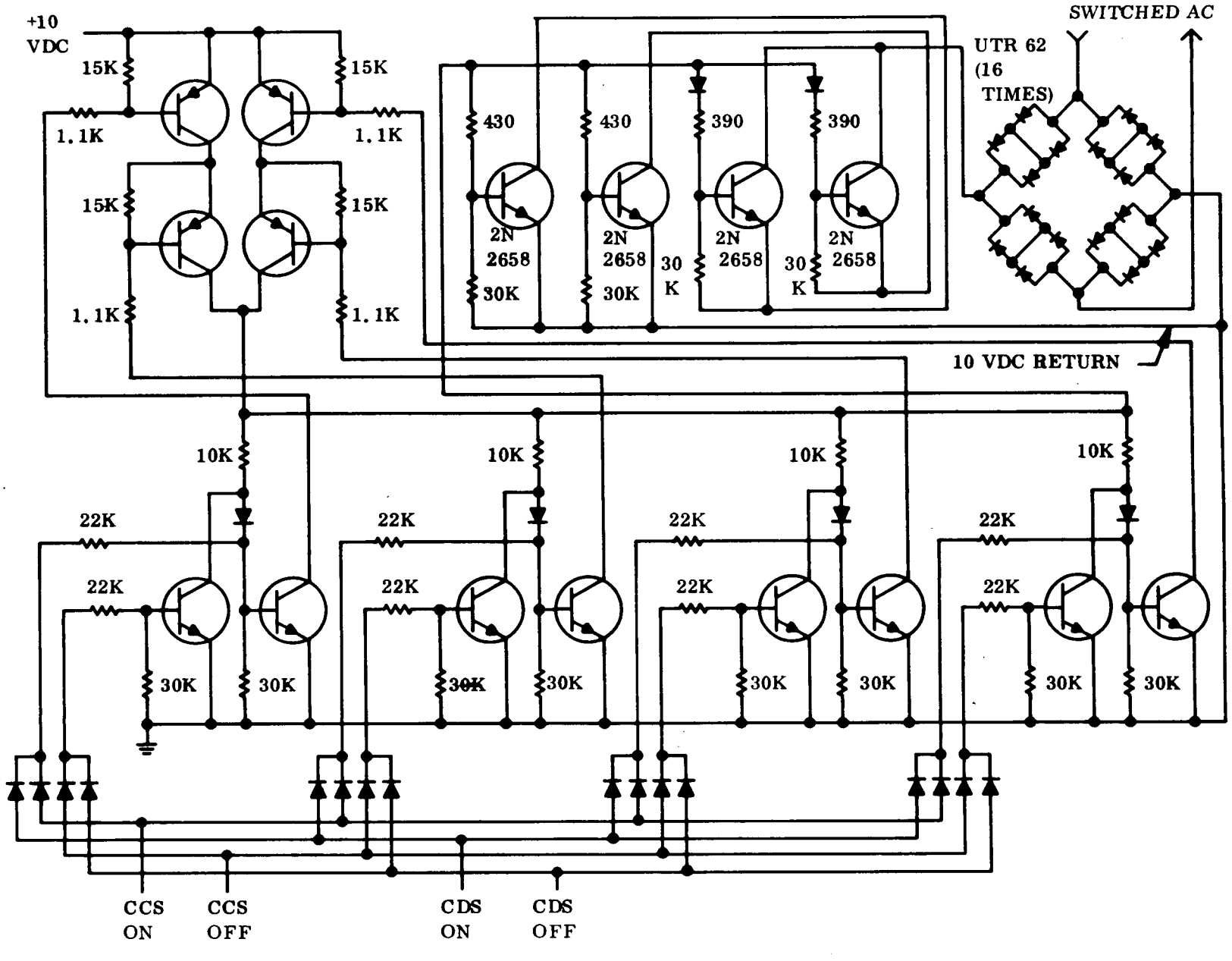


Figure 5.9-14. Transistor Switch Schematic

This circuit is connected directly to the ac power lines. To maintain ground isolation a dc power supply is required for the switch control circuits. Ten volts was selected to reduce power loss in the dc circuits.

5.9.3.2 Test Results

Figure 5.9-15 shows the relatively large magnitude and change in the voltage drop across this switch. This represents both a power loss and regulation degradation. Figure 5.9-16 summarizes the power losses in the switch. Since the current switch must control the full load current, the dc drive and control current is quite large and causes a large power loss, much larger than the voltage drop losses in the ac line. Taking into account all switch losses (but not the loss for the dc power supply) the ac power delivered divided by all input power is given in Figure 5.9-17. While it would appear that simply loading the switch more would yield higher efficiency, this would violate the forced beta design for the pass transistors. Since the design is for a very long life and harsh environment, this cannot be done and the 225 Ω curve must be accepted as a reasonable upper limit of efficiency for this design.

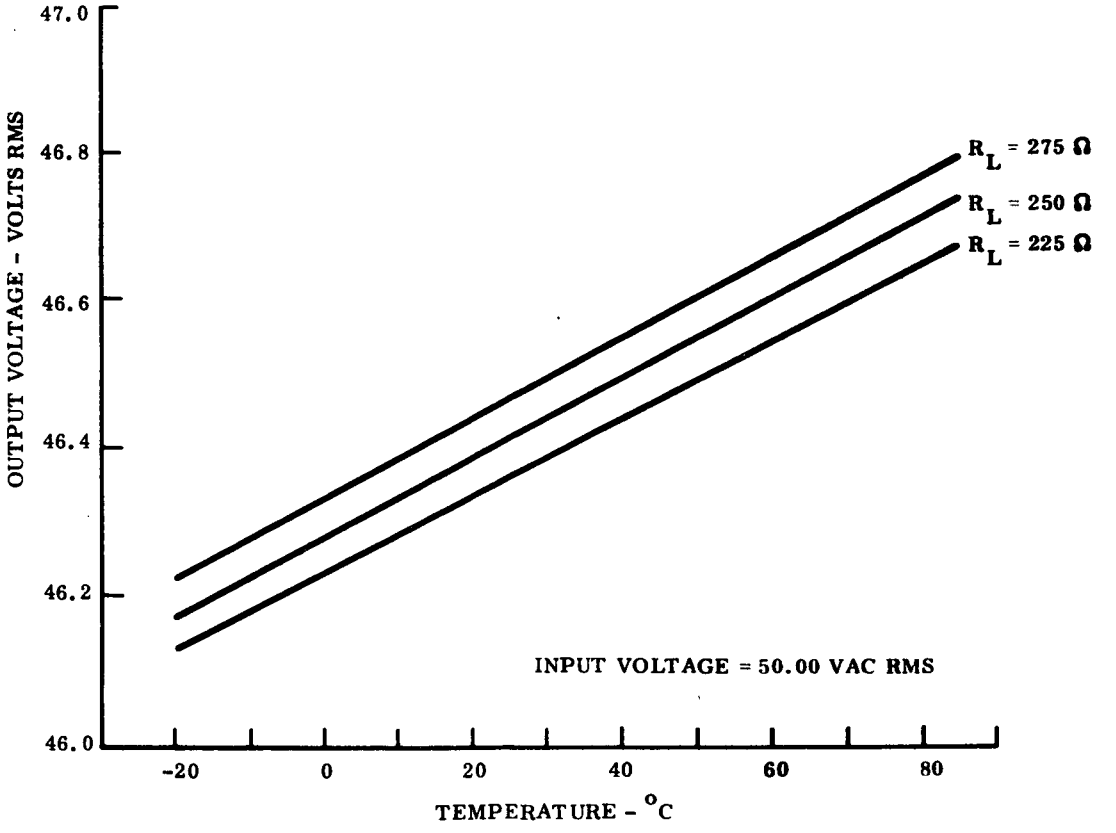


Figure 5.9-15. Solid State AC Switch No. 1 (10 Watt) Output Voltage

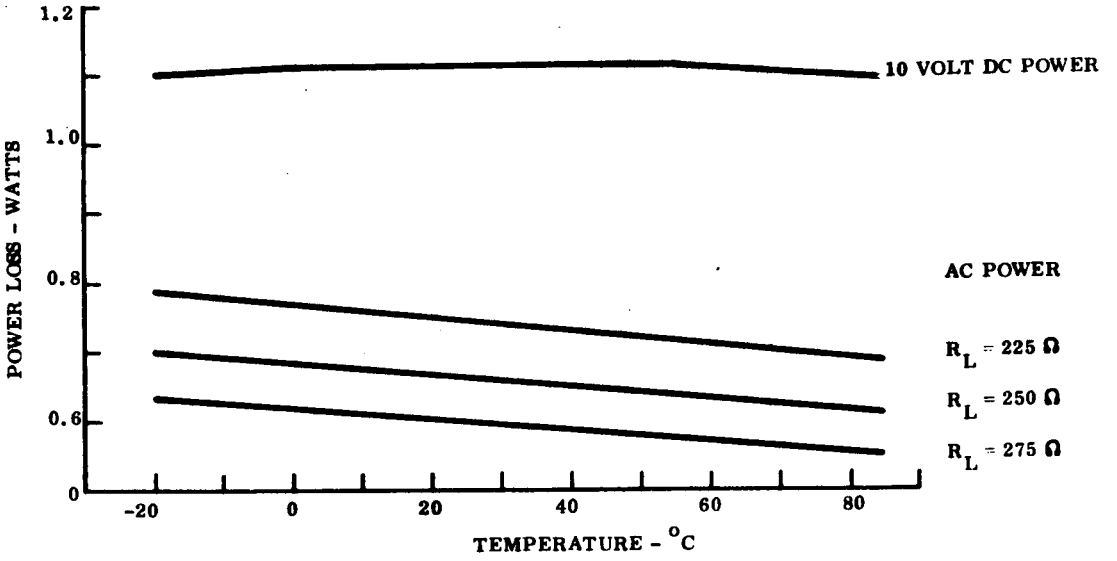


Figure 5.9-16. Solid State AC Switch No. 1 (10 Watts) Power Losses

A special ambient test was performed to determine the interaction between two transistor switches. Two setups were devised to operate two switches from a single dc source. Setup No. 1 of Figure 5.9-18 references the return of the dc supply indirectly through the diode bridge to the inverter. Setup No. 2 of Figure 5.9-19 references the dc supply directly to one side of the ac inverter.

In Figure 5.9-18, switch No. 1 is on and switch No. 2 is off during the first half cycle of the inverter. The dc voltage across each switch control circuitry (Vss) is approximately 10 volts when the polarity of the inverter changes at the second half cycle, the return side of the dc

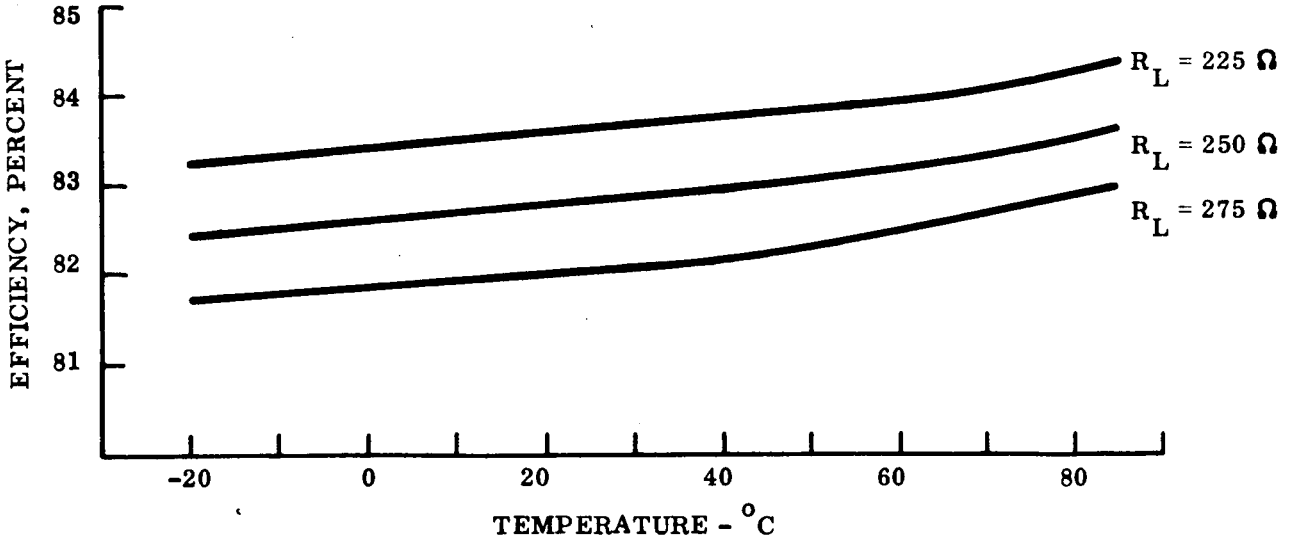
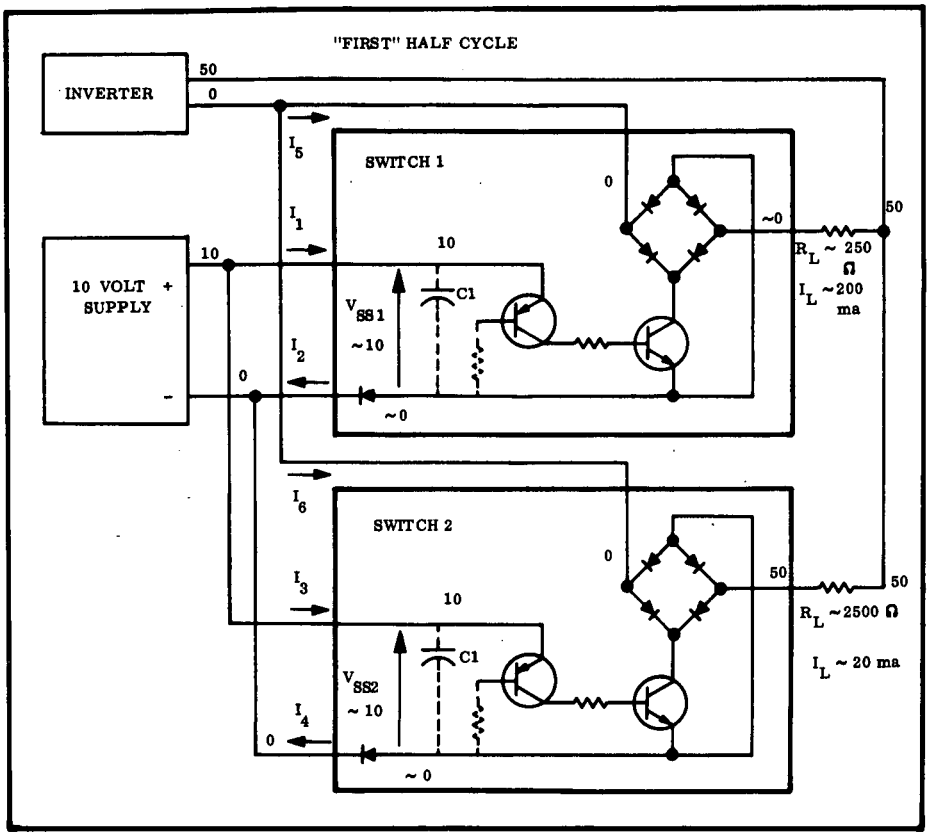


Figure 5.9-17. Solid State AC Switch No. 1 (10 Watts) Efficiency



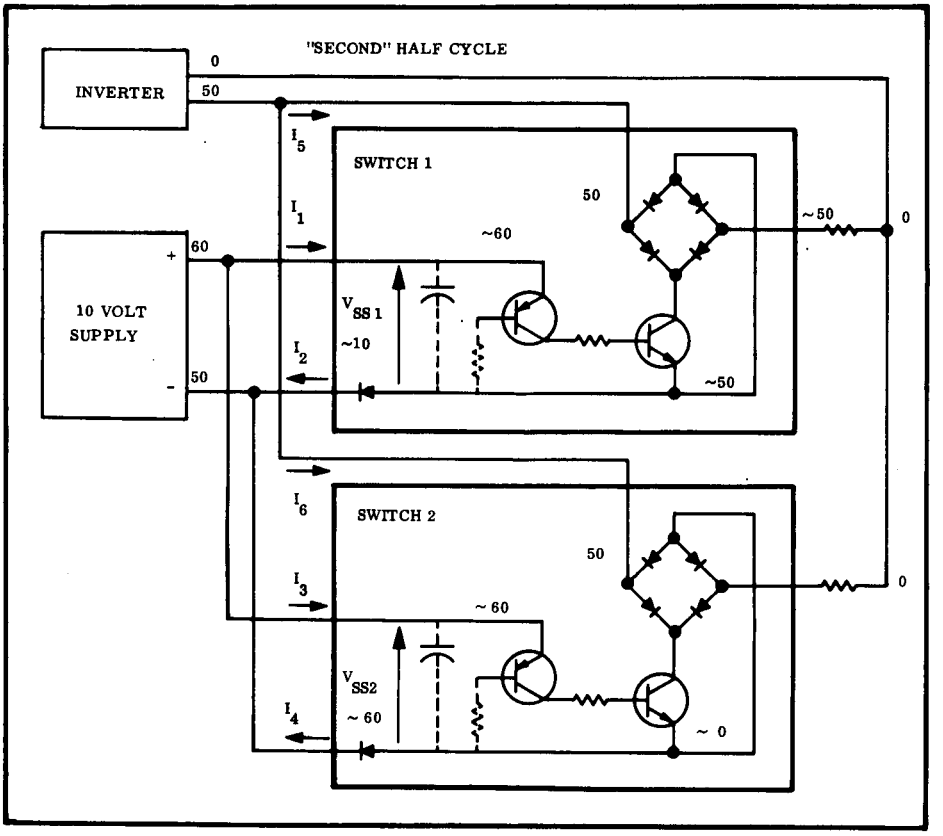
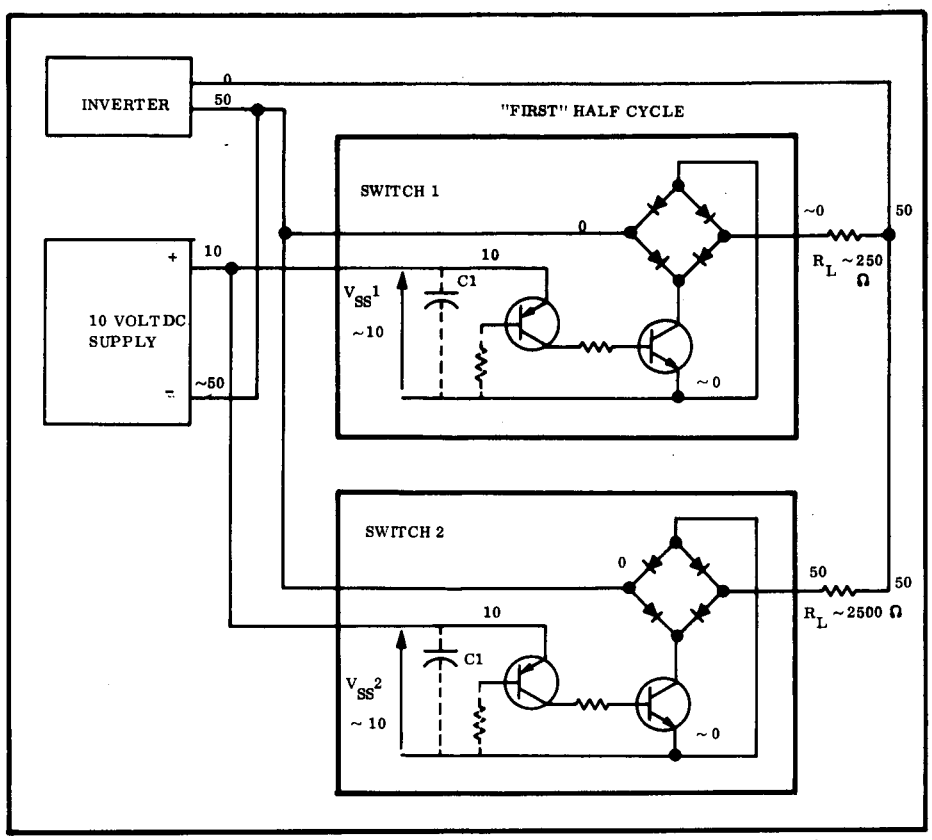


Figure 5.9-18. Transistor Switch Test Setup 1



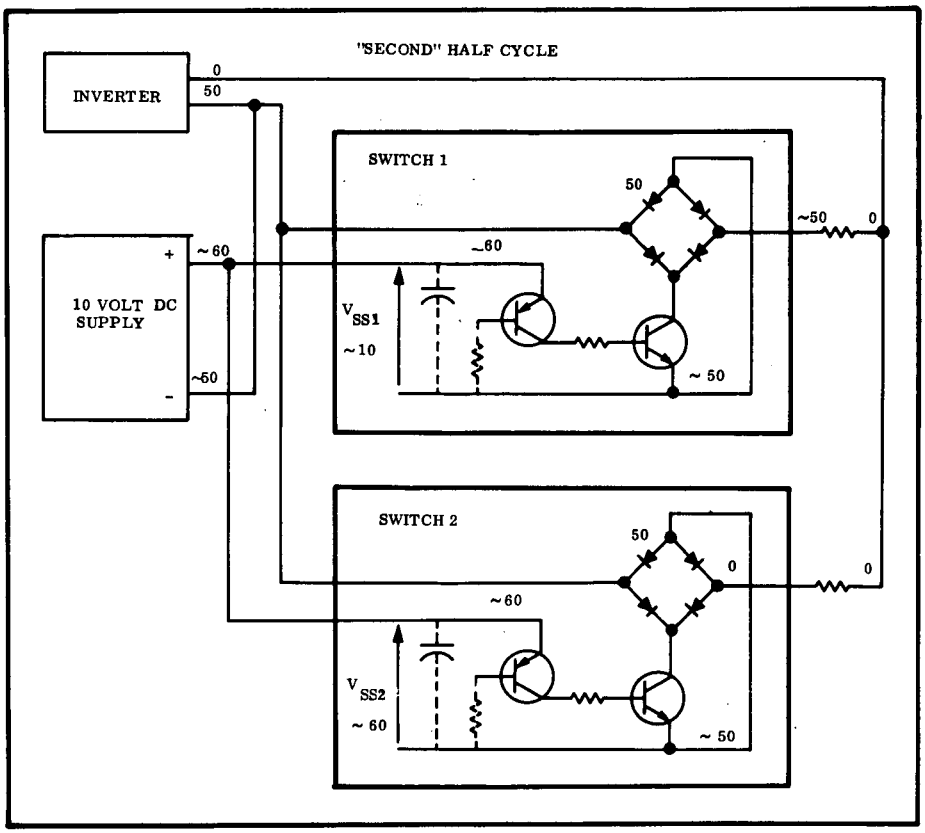


Figure 5.9-19. Transistor Switch Test Setup 2

supply floats up to about 50 volts. As a result, about 60 volts is impressed across the control circuitry of switch No. 2 (Vss2). This step causes turn on of switch No. 2 due to transistor and stray capacitance of the switch. Placing a capacitor (C1) across Vss of each switch causes the voltage to change slow enough to prevent premature turn-on. However, the ac current through the capacitor is quite large. This same situation exists for Setup No. 2 of Figure 5.9-19.

Another problem exists when both switches are ON. Figure 5.9-20 shows the wave forms of various currents in Setup No. 1. These wave forms will be used to show that the currents change path with each half cycle and take the path of least resistance.

Referring to Figure 5.9-20, currents into the switches I_1 and I_3 maintain constant magnitudes during each half cycle of the ac load currents. Their return paths, I_2 and I_4 however, are changing in magnitude with each half cycle. Also note the variations in ac currents I_5 and I_6. This shows that some of the dc control current is returning to the dc power supply via the ac lines common to the two switches. As a result, the pass transistor of switch No. 2 is controlling much more current than it was designed for. This shifting of currents from the desired path was also evident in Setup No. 2. Another problem created by this half cycle imbalance is generation of electromagnetic interference.

The 10 volt supplies must float on the ac line, also an EMC problem and a command source problem. Finally, a capacitor across Vss or much lower impedance command and control electronics is needed to prevent spurious turn on. The former causes current spikes (seen in I_1 and I_3 of Figure 5.9-20 and the latter higher power consumption).

Another alternate of using separate dc power supplies for each switch would eliminate this problem, but is not considered a practical solution due to the large number of switches required in the power subsystem. Due to the above complications and the rather low efficiency, no further work was done on this type of switch since it seemed inapplicable as a general application switch for the TOPS power distribution.

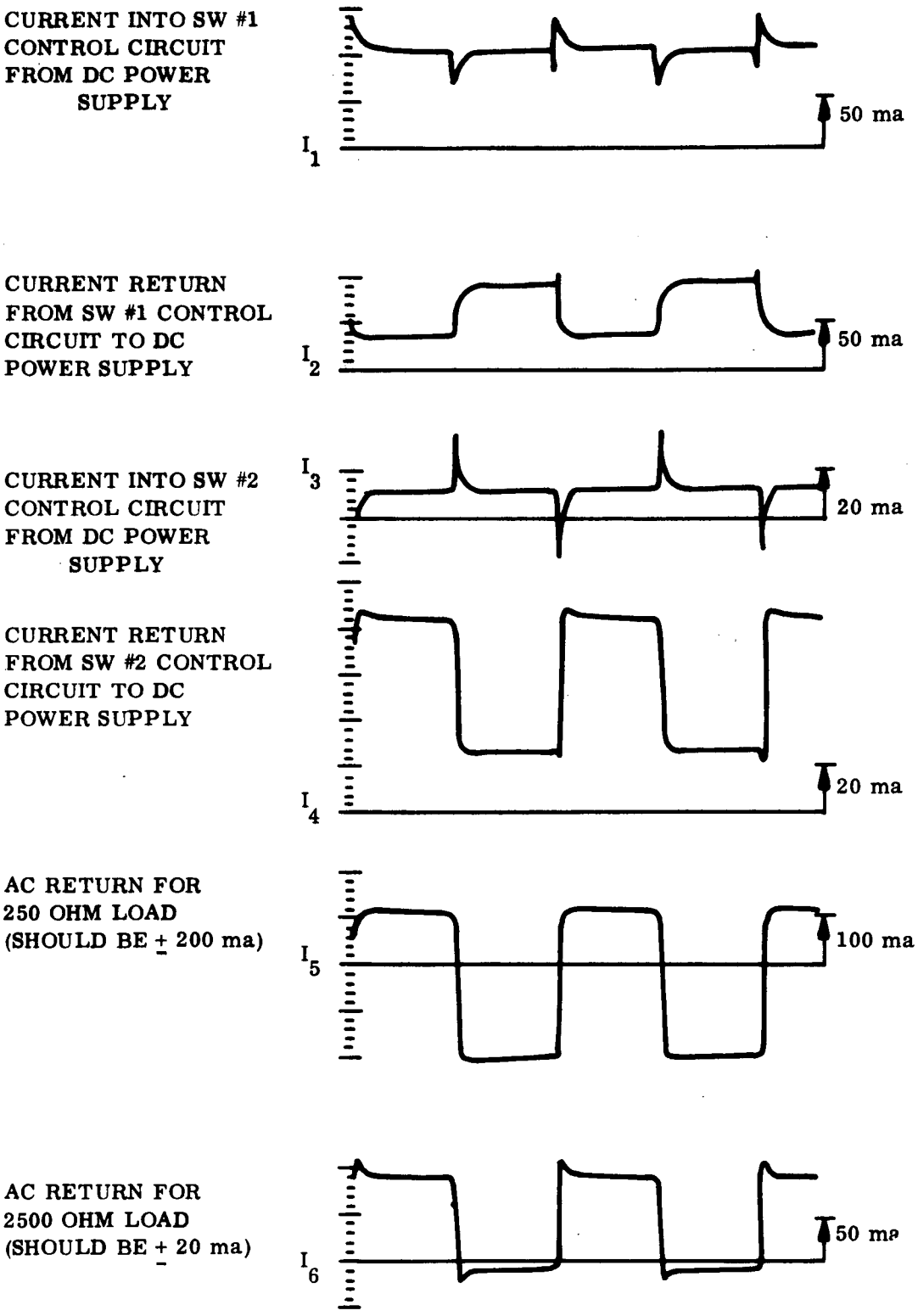


Figure 5.9-20. Setup No. 1 Transistor Switch Currents

5.9.4 AC CURRENT LIMITER

5.9.4.1 Design Description (Figure 5.9-21)
The requirements, for which a specific design was made, were to limit ac current passed to less than 1.8 amps. The limiter must pass 45 watts (0.9 amp) at 90% or better efficiency.

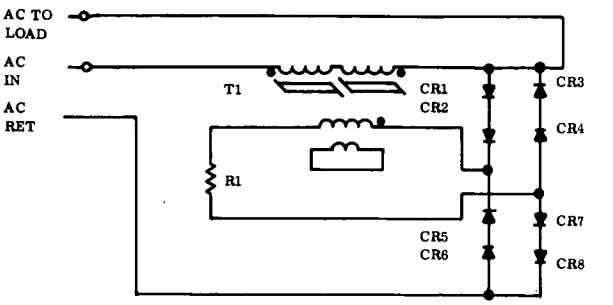
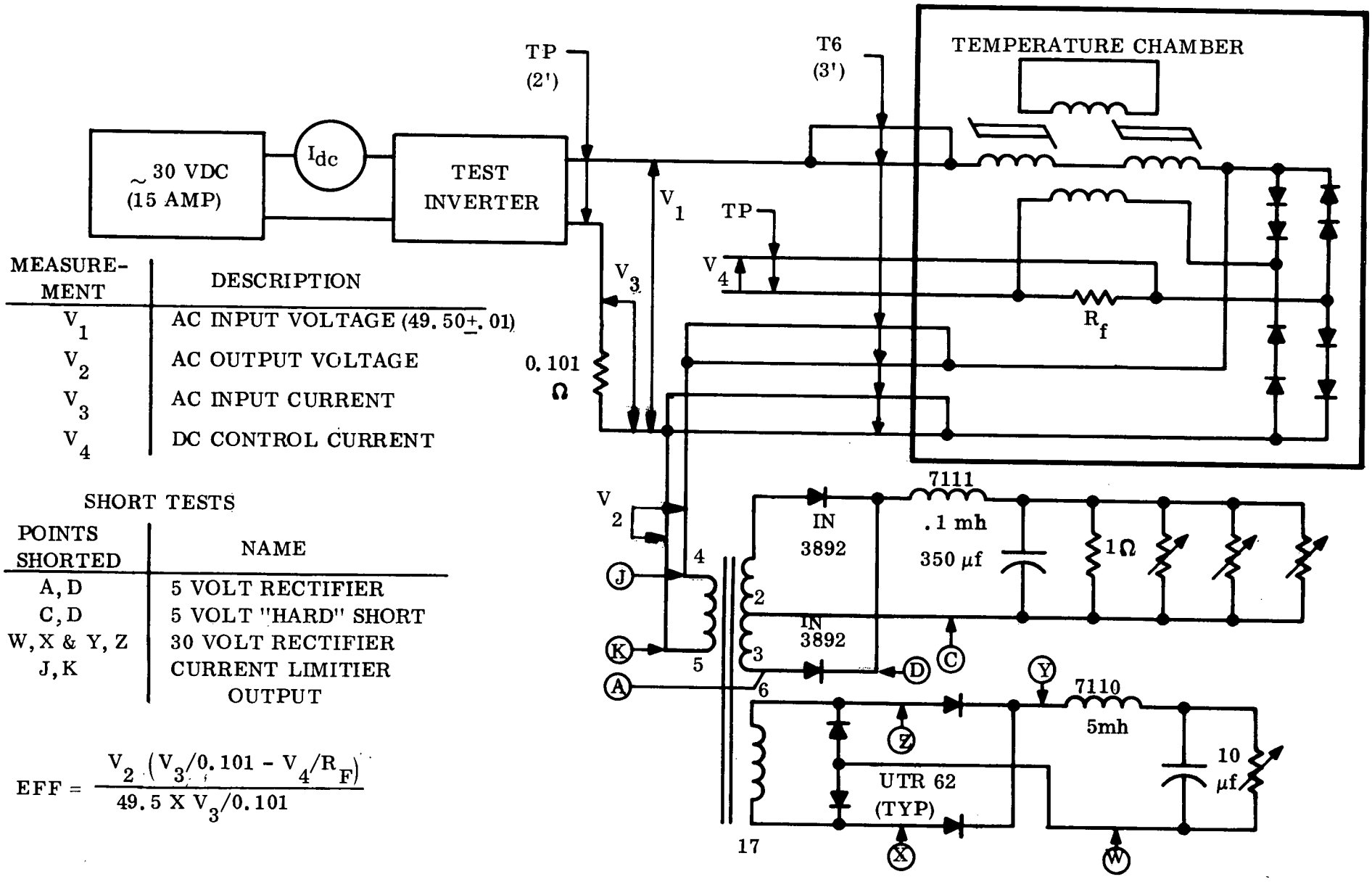


Figure 5.9-21. AC Current Limiter Schematic

The design utilizes two saturable reactors which are biased by a common control winding. Using the output to provide the control current provides a "fold back" characteristic, which means the power delivered to the load actually decreases as load resistance decreases. When the ampere turns in the gate winding (power path) exceed the control current, the inductor comes out of saturation and supports part of the voltage, hence limiting the current drawn by the load. When one gate winding is supporting part of the voltage and limiting the current, the supported voltage is reflected in the control winding (a much larger voltage) and causes a large increase in control current; hence, the limit current is considerably greater than 1.8 amps for low resistance loads. The duty cycle is short however because the large amount of volt seconds put into the core must be taken out in the next half cycle. Until the core saturates all the applied voltage is supported and no current flows. The shorted turns around the two cores causes both cores to share the supported voltage while no current is passed. The "harder" the overload, the more volt seconds are applied each half cycle, which causes a shorter duty cycle and a reduction of input power. Of course, the current spikes each half cycle must be tolerated by the ac source.

An approximate 50:1 ratio was chosen for the control current. This corresponds to a 4% loss due to control current alone, since the limit is set at twice the operating current. The higher the ratio, the greater the current spike will tend to be when limiting.

5.9.4.2 Test Results
The test setup is given in Figure 5.9-22. A transformer/rectifier (TR) was used to load the limiter. The overload condition was caused by reducing the dc loads. Hard shorts were applied by a 6 inch clip lead across the points indicated in the matrix. Each unit was tested -20, 0, 25, 55, and 85°C.



MEASURE-MENT	DESCRIPTION
V_1	AC INPUT VOLTAGE (49.50±.01)
V_2	AC OUTPUT VOLTAGE
V_3	AC INPUT CURRENT
V_4	DC CONTROL CURRENT

SHORT TESTS

POINTS SHORTED	NAME
A, D	5 VOLT RECTIFIER
C, D	5 VOLT "HARD" SHORT
W, X & Y, Z	30 VOLT RECTIFIER
J, K	CURRENT LIMITIER OUTPUT

$$EFF = \frac{V_2 \left(V_3/0.101 - V_4/R_F\right)}{49.5 \times V_3/0.101}$$

Figure 5.9-22. AC Current Limiter Test Set Up

Preliminary testing included evaluation of a 25:1 ratio unit for comparison of limiting characteristics to the 50:1 design.

Figures 5.9-23 and 5.9-24 present the efficiency results for the first (breadboard) and second (qual) test units. The first unit loading was slightly less than the 45 watt desired nominal which results in the generally lower efficiencies at 34 and 37 watts. However, the control current was a bit low, which caused the 41 watt efficiency to be higher than the qual unit 42 watt efficiency. The copper losses at 48 watts and high temperature cause the lowered efficiency seen in the qual unit. The efficiency adequately exceeds the 90% requirement.

Figures 5.9-25 and 5.9-26 show the voltage loss due to the current limiter. The qual unit had a higher voltage drop corresponding to the heavier loading. The -7 to +7% load change and temperature cause a 1.3% change in voltage (out of 50) or degradation in regulation. The maximum drop corresponds to a 3% loss of voltage.

Figures 5.9-27 and 5.9-28 give the amplitude/width results as the load resistance was decreased for each output of the TR. These results are for the quasi square wave current which is the passed current waveform when limiting occurs. Low temperature always produced the highest amplitudes. Since the 30 volt output represents a "harder" short (due to the voltage contribution of rectifiers in the 5 volt output), an overload there produced the minimum durations. Some variation in characteristics can occur among different units, as seen in these results, due to slight differences in the construction and magnetic properties. For reference, Figure 5.9-29 shows the overload results for the 25:1 (control to gate) ratio design.

Figures 5.9-30 and 5.9-31 present the results of short tests indicated in Figure 5.9-22. The current waveform is a current "spike" each half cycle, as depicted in Figure 5.9-30. The circled data point represents the $-20^{\circ}C$ test. As with the overload characteristics, the qual unit limited better. The 25:1 ratio unit was a little worse than the 50:1 qual unit. The short and overload results of the 25:1 unit were not greatly better than any 50:1 unit, so the higher ratio seems better, since it is 4% more efficient.

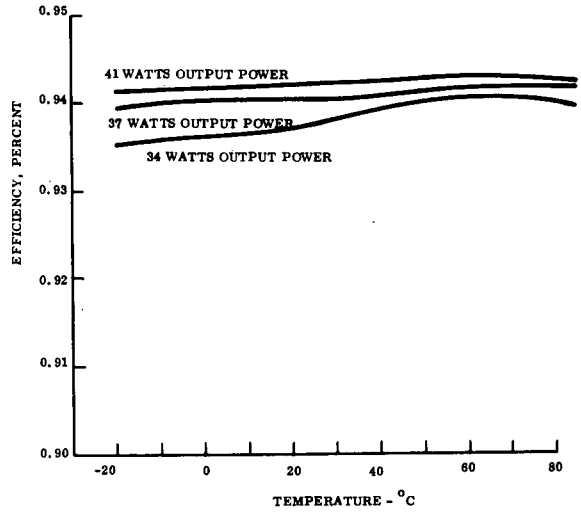


Figure 5.9-23. AC Current Limiter Breadboard Efficiency

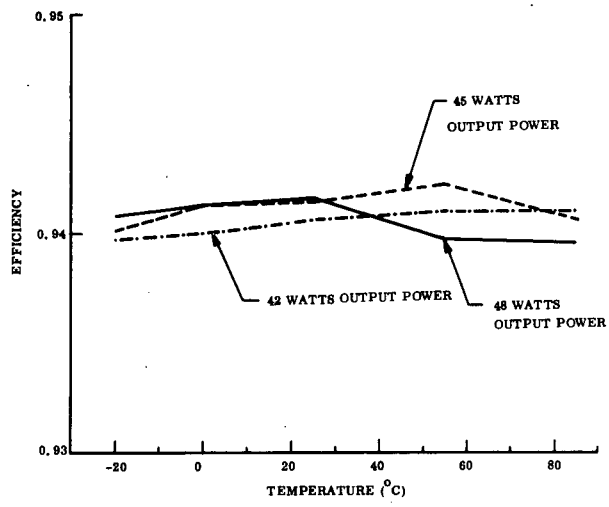


Figure 5.9-24. AC Current Limiter Qual Unit Efficiency

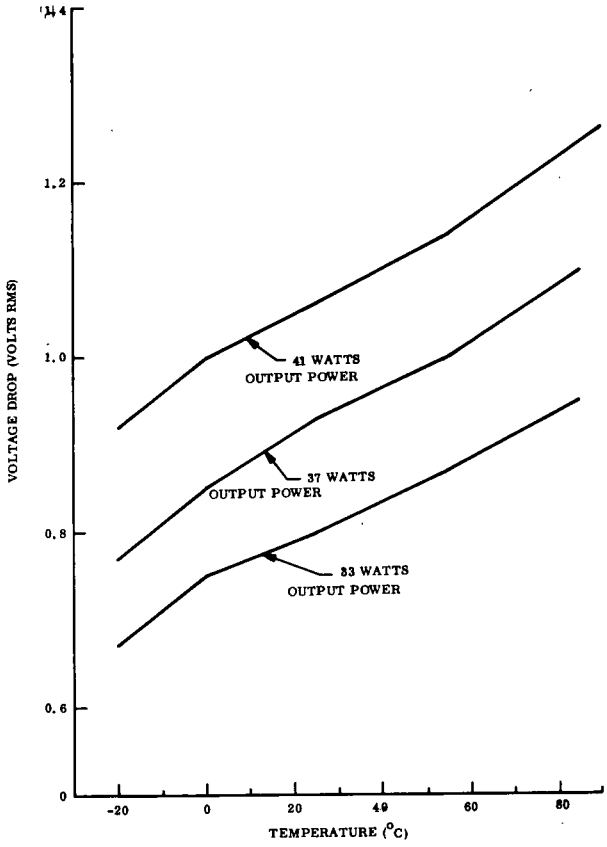


Figure 5.9-25. AC Current Limiter Breadboard Voltage Drop

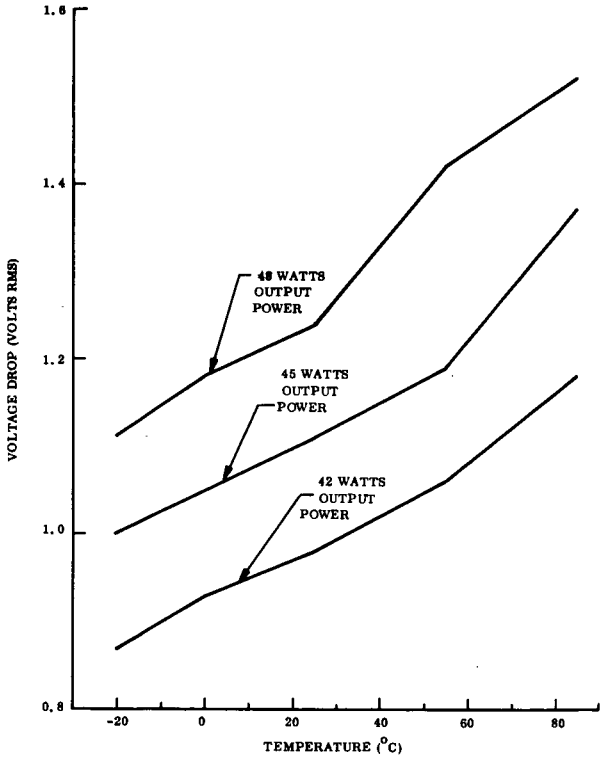


Figure 5.9-26. AC Current Limiter Qual Unit Voltage Drop

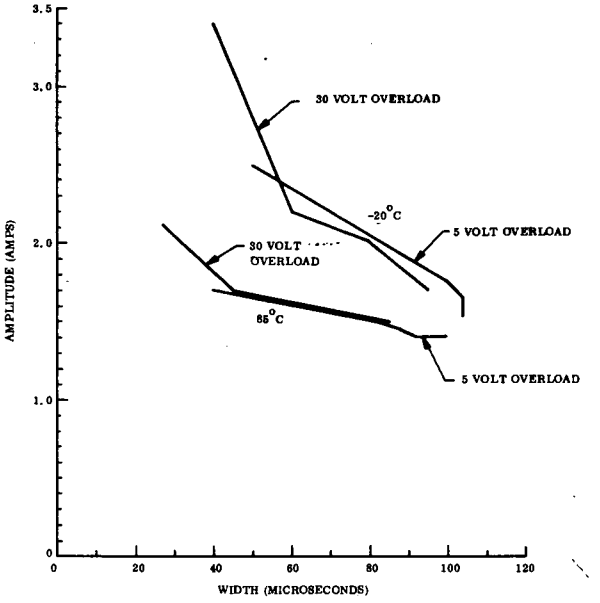


Figure 5.9-27. AC Current Limiter Breadboard Overload Characteristics

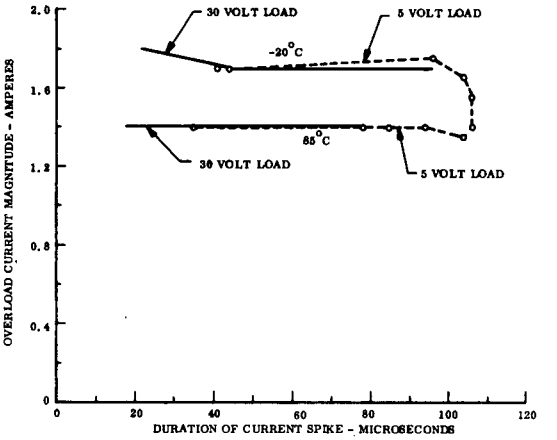


Figure 5.9-28. AC Current Limiter Qual Unit Overload Characteristics

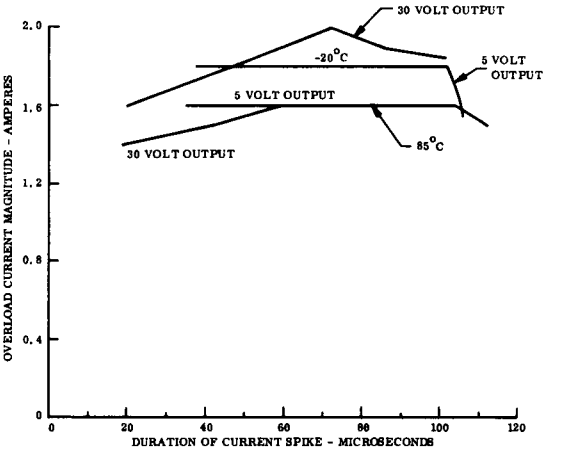


Figure 5.9-29. 25:1 AC Current Limiter Overload Test Results

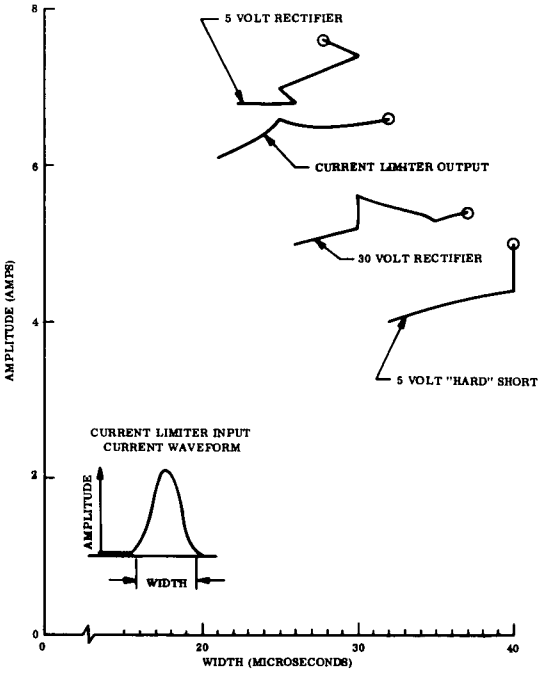


Figure 5.9-30. AC Current Limiter Breadboard Short Tests

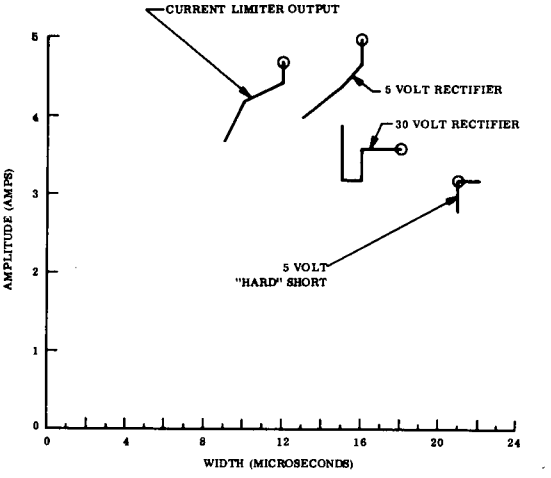


Figure 5.9-31. AC Current Limiter Qual Unit Short Tests

Figure 5.9-32 gives the power limiting characteristics of the limiter for increasing overload. Figure 5.9-33 shows the input power under various short conditions. The fold back characteristic is seen on these two figures, the power is lowest at the "hardest" output short (the current limiter output).

5.9.4.3 Failure Mode, Effect, and Criticality Analysis

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.9-4. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

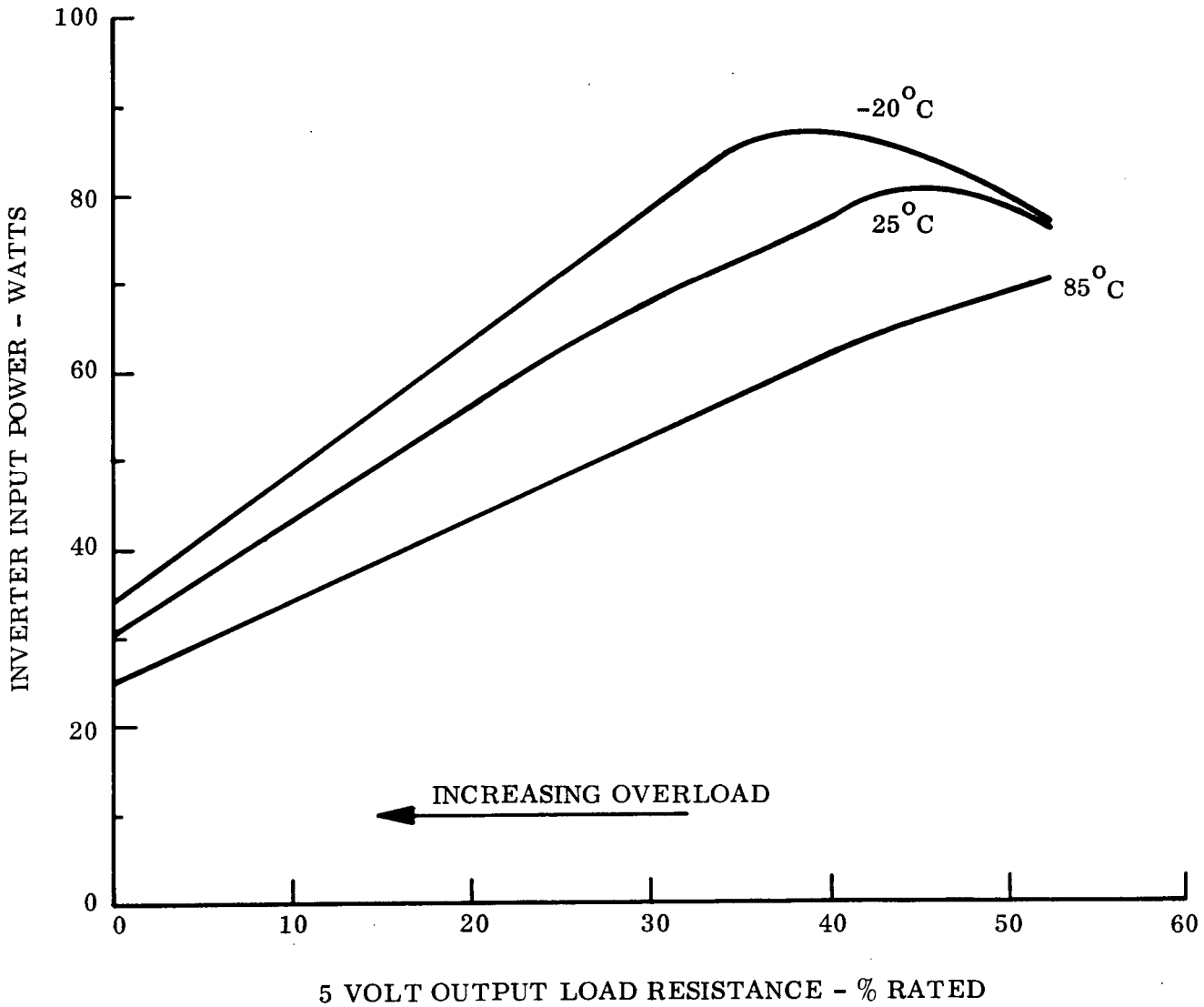


Figure 5.9-32. Inverter Input Power for AC Current Limiter Qual Unit - 5 Volt Output Overload

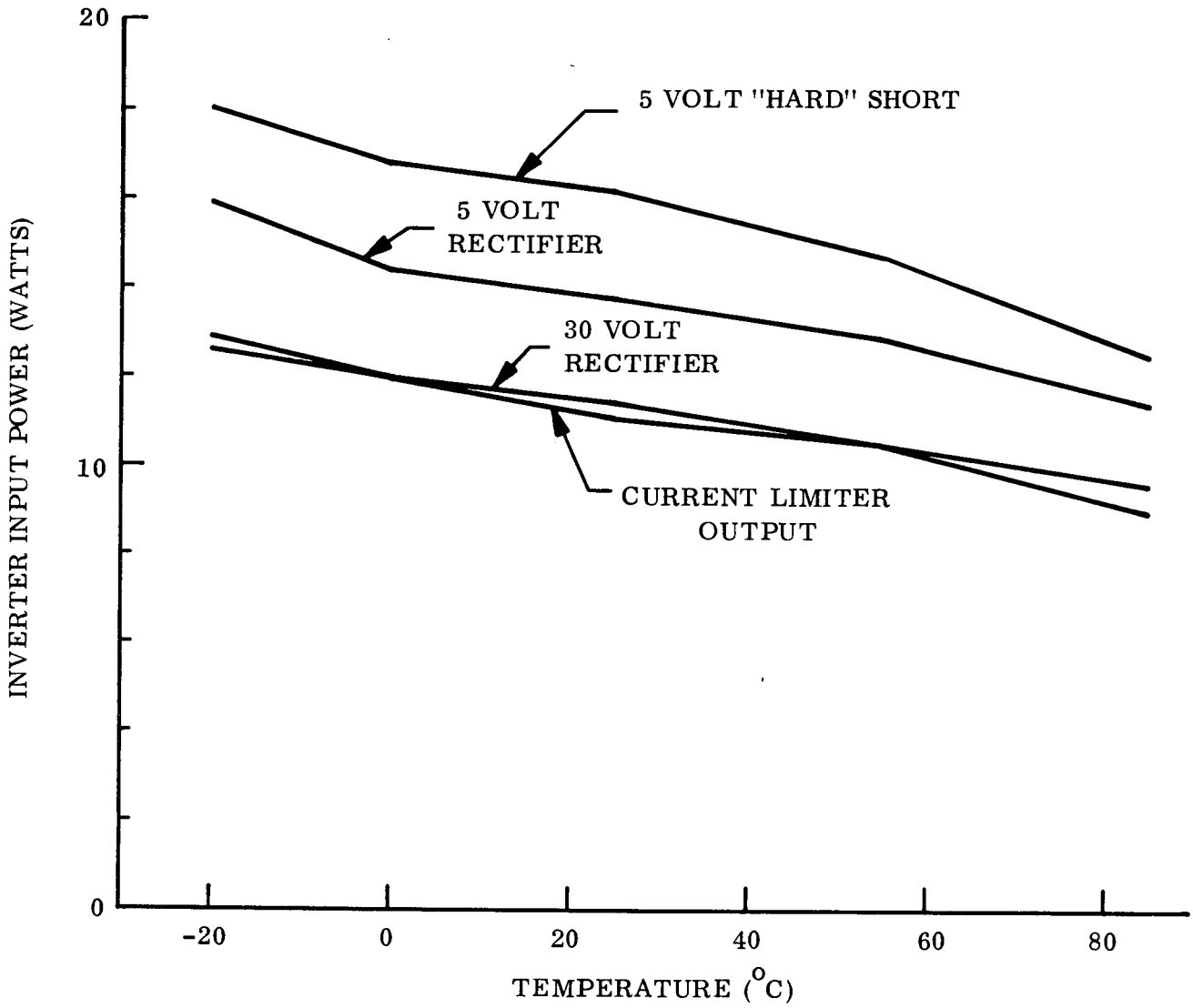


Figure 5.9-33. AC Current Limiter Qual Unit Shorts - Inverter Input Power

Table 5.9-4. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component A.C. CURRENT LIMITER
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	T1	Mag Amp.	Supports the source A.C. voltage during a portion of each half cycle in order to limit the average current to an overload.	Open Gate Winding and Open or Short Control Winding		Loss of DC control current or open circuit to the load	The load would turn off.		Winding 1-2 supports the voltage during the first half cycle. Winding 3-2 supports the second half cycle. Winding 4-5 provides the control ampere turns.
				Short Gate Winding		Reduces the duration in which the gate windings(power path to the load) can support the source voltage.	Allows more average current to flow into a failed load.		
2	R1	Resistor	Limits the current in the DC control winding	Open		Control winding would be open circuited. Windings 1-2, and 3-2, would support the AC source voltage.	The load would turn off.		
3	CR1	Diode	Provides control current which is proportional to the voltage across the load (gives foldback characteristic)	Open		Control winding would be open circuited. Windings 1-2, and 3-2, would support the AC source voltage.	The load would turn off.		

Table 5.9-4. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component A.C. CURRENT LIMITER
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
3				Short		NONE		CR1 is backed up by series redundant CR2.	
	NOTE:	Diodes CR2 thru CR8 have the same failure modes and effects as CR1 above.							

5.10 LOW VOLTAGE CUT OFF (LVCO)

5.10.1 FUNCTIONAL REQUIREMENTS

The Power Subsystem is primarily dependent upon CCS for load fault detection and correction. The LVCO provides a backup function within the Power Subsystem to protect against a long time low voltage condition on either the ac or dc Main Bus in the event that CCS fault correction capability is lost. The LVCO senses the ac Main Bus voltage, 50 vrms + 3-4 percent, at the output of an inverter. If an undervoltage condition appears, that is, the bus voltage is reduced to 45 ± 1 vrms, for a finite period of time (T1), the LVCO will then immediately send an interrupt signal to CCS. The existence of the interrupt signal will be for the duration of the undervoltage condition. This interrupt signal will be a steady state command that is reset by restoration of the Main Bus voltage. This signal will be hard wired to CCS and will be synchronous with a 500/ 9 KHz externally supplied clock pulse 1.5 ± 0.5 μs wide. The interrupt signal informs CCS that the Power Subsystem intends to change the state of the spacecraft loads within a fixed time (T2) unless stopped by either removal of the system fault (returning the bus voltage to specification) or a CCS inhibit command to the LVCO. If not stopped, the LVCO will then remove all non-critical loads. If, after this action, the Main Bus voltage still does not return to spec within a preselected time (T3), the LVCO will then transfer all critical loads (those loads required for establishing a command up-link to receive ground commands) to their standby units. At any time during the period T1 through T3 the LVCO will be capable of receiving an inhibit command via the "S/ C Command Data Bus" from CCS, if it is determined by CCS that the Main Bus is within specification. This inhibit would stop all further action by the LVCO. If, at any time after a low voltage condition occurs, the Main Bus returns to spec, the LVCO will cease further action and return to its standby state. The LVCO will contain sufficient energy storage to operate one time after the loss of Main Bus power.

5.10.2 DESIGN DESCRIPTION (FIGURE 5.10-1))

The main ac bus voltage is sampled, and power supplied to the LVCO by a 1:1 transformer. The approximate 46 volts dc obtained by rectifying and filtering is used for energy storage to minimize capacitor size. A series regulator (CR 10 and Q1) provides a relatively precise lower voltage for the detector (LM101) and timing divider. This also helps reduce capacitor

FOLDOUT FRAME 1

FOLDOUT FRAME 2

FOLDOUT FRAME 3

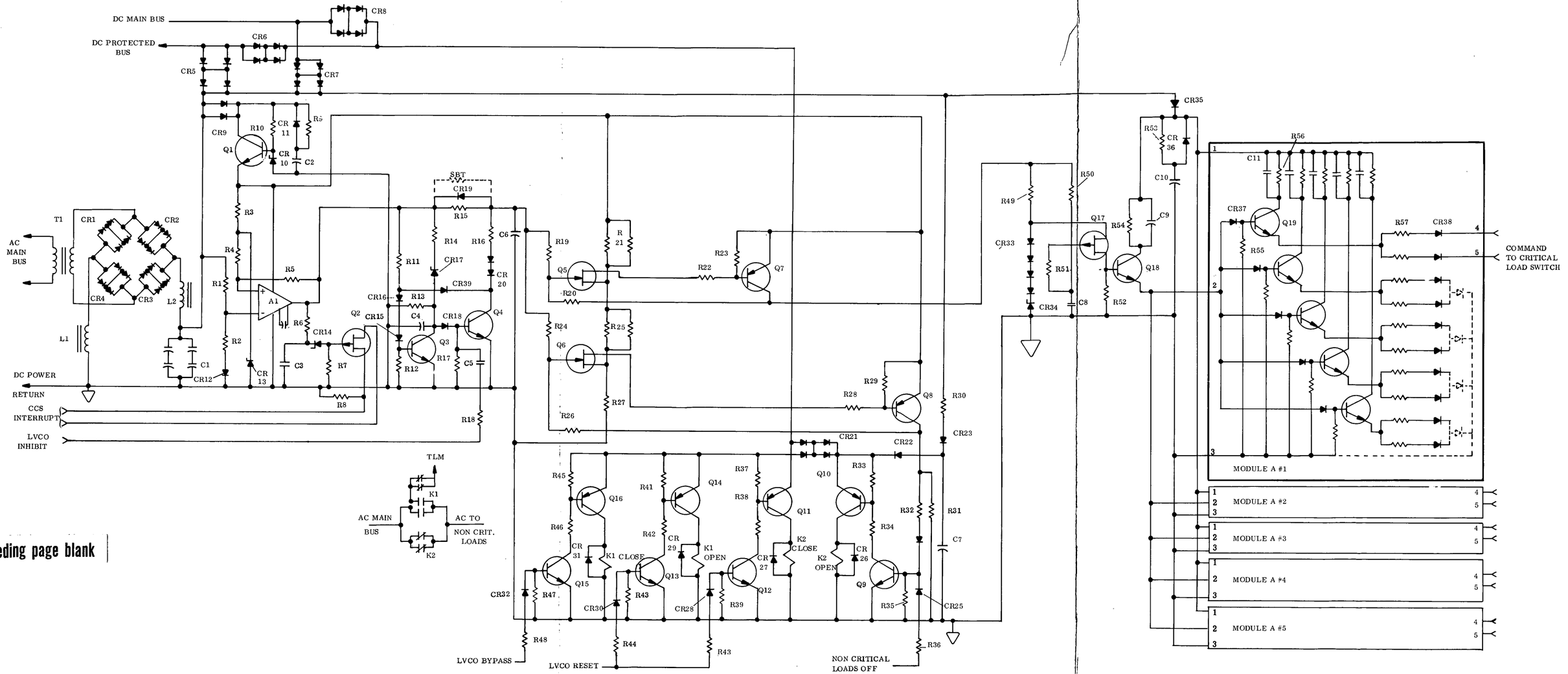


Figure 5.10-1. LVCO Schematic

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5-232

capacity since these loads become constant current. The ac voltage is compared against a reference (CR 13) by a voltage divider which is temperature compensated by the diode of the same type used in the rectifiers. An FET switch with a short delay is used for generating an impedance change which can interface to TTL circuits for the CCS interrupt signal.

The other outputs are originated by two FET switches biased at different voltages by a resistor divider. The op amp output charges a capacitor (C6). The capacitor voltage ramp is applied to the FET gates and each turns on when its gate-source voltage rises above its pinch off. The FET drain current is kept small to minimize its effect on the voltage divider. Timing ceases and the capacitor is quickly discharged in the event the ac voltage returns to normal.

A two transistor self-latching curcuit is used to short the timing capacitor if an inhibit command is received when the op amp is high. The circuit remains latched on, shorting the timing capacitor, which prevents all outputs, until the op amp output returns to a low state. A command received when the op amp output is low has no effect. The inhibit command is capacitive coupled to prevent incorrect inhibiting of the outputs due to a failure of the command circuit, since that failure is impossible to detect until it is too late.

Relays K1 and K2, with their drivers, make up a switch for an ac/ dc bus for powering all noncritical loads. Both relays can be opened and closed by CCS for its use in power control or fault clearing. The LVCO can open K2, which is the relay normally used to provide noncritical load power. K1 should only be closed if K2 cannot be closed.

The output of the timer and amplifier for T3 (Point A) is applied to a voltage reference (CR 33 and CR 34) for a two stage emitter follower output. An FET switch (Q17) limits the pulse width of the output to be compatible with the present Power Distribution Switch. The emitter follower outputs and single driver provide the current gain required and full isolation of the output to each switch. Capacitors in the output transistor collectors prevent continuous application of a command to any switch due to any single part failure. This must be done to prevent locking any switch in one position due to an LVCO failure. Placing the capacitors in the collectors rather than in the output line minimizes capacitor size because a rather large charge buildup

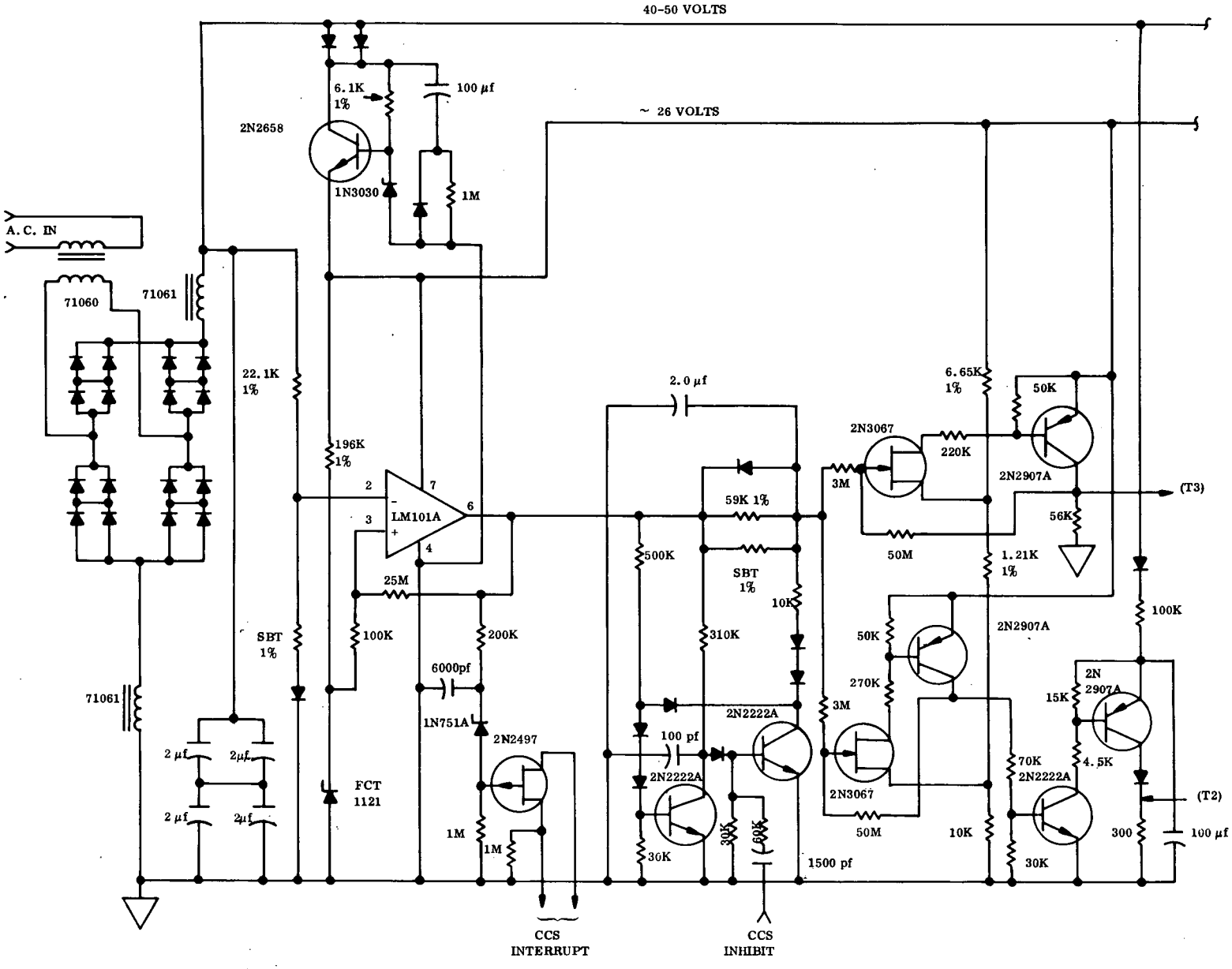


Figure 5.10-2. LVCO Breadboard Unit Schematic

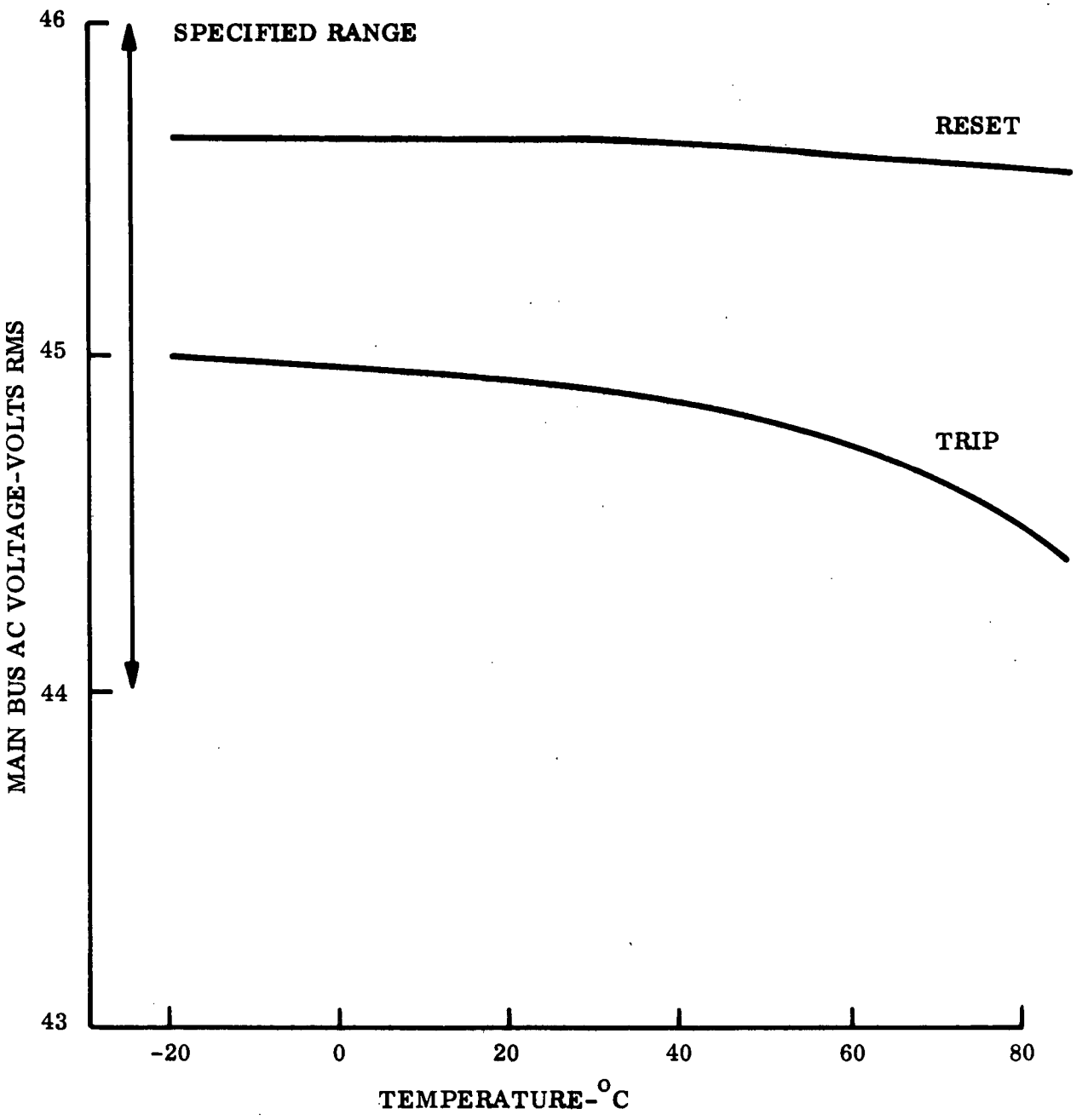


Figure 5.10-3. LVCO Breadboard Unit Trip Voltage

The photographs also show pulse width of the outputs and, to some extent, the energy storage duration.

The circuit was tested in various modes, such as with the dc supplies turned off, and a trip caused by switching off the ac to prove energy storage adequacy. The circuit was also tested by allowing all capacitors to discharge by removing all power and then quickly reapplying all power and switching off the ac again. This prevents the energy storage capacitors from charging and demonstrates that the circuit will operate from the protected bus without energy storage.

Real relays were used in the noncritical load bus control so the T2 function could be adequately demonstrated. To prove the adequacy of the T3 switch drive output, the interface was simulated using properly loaded transistors, (2N2222A, typically), thus duplicating the first stage of each load switch. The specifics are given in Figure 5.10-4. The base current was measured between the base emitter resistor and the base as shown, therefore it is the true base current. The current was measured using a 100 turn coil and dc current probe. Though the coil-probe combination was calibrated for each set of data, the overall accuracy of these measurements can be as much as ± 5 percent due mainly to possible reading error.

Five output transistors of T3 (one in each module A) were shorted, base-to-emitter, to demonstrate the failure tolerance of the driver. The outputs monitored in T3 were selected such that outputs with shorted transistors were monitored as well as normal outputs.

The ac input current was measured using an ac current probe and oscilloscope.

Figure 5.10-5 presents the trip and reset results for the qual unit. In the bridge rectifier, several diodes could short and near correct operation would continue. The graph shows that one short in each location in the bridge would lower the trip point out of the specified range. Such an event is most unlikely, but the loss of two diodes to a short should be allowed in assessing the LVCO reliability since this will not lower the trip point below the specified range.

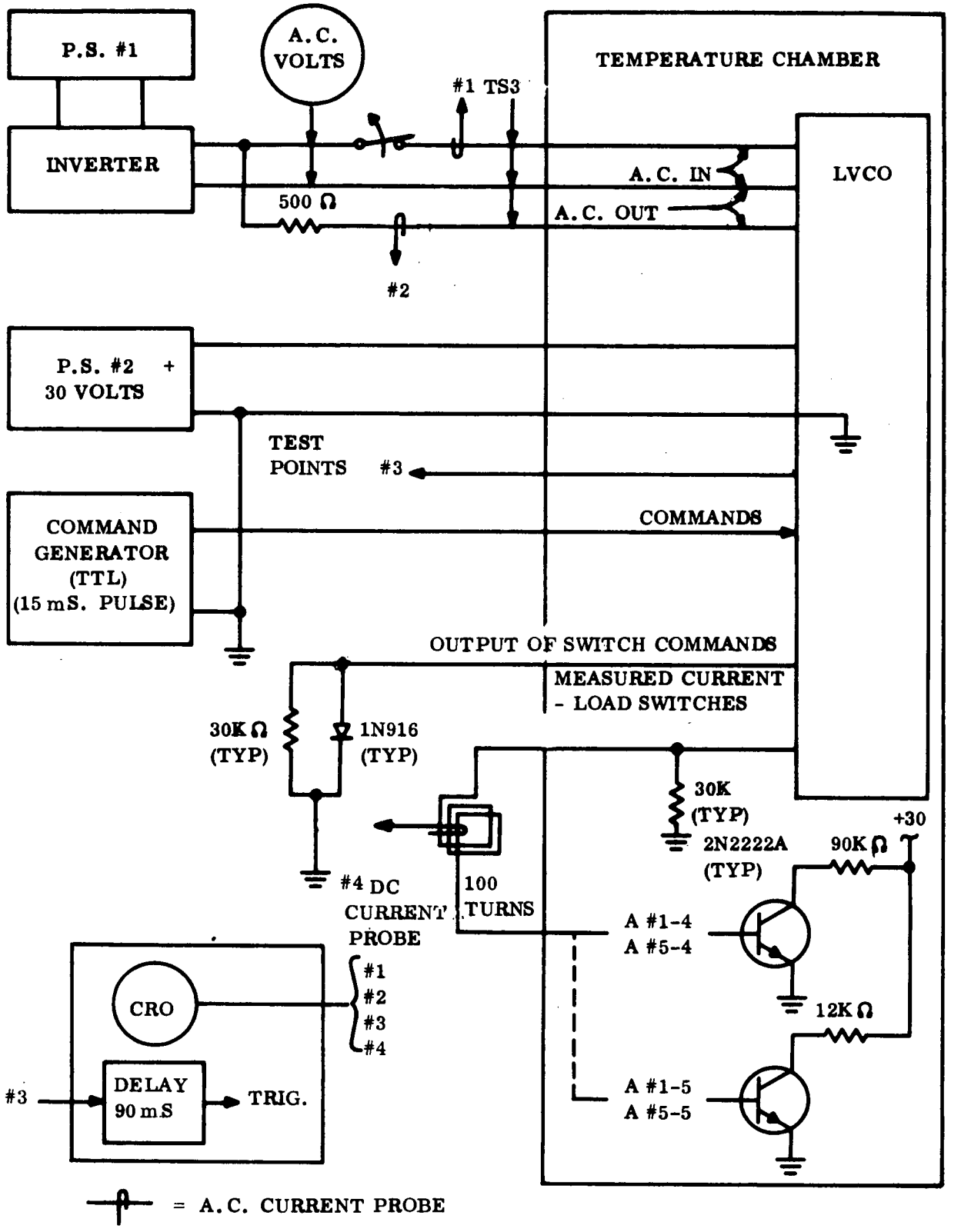


Figure 5.10-4. Qual Unit Test Set Up

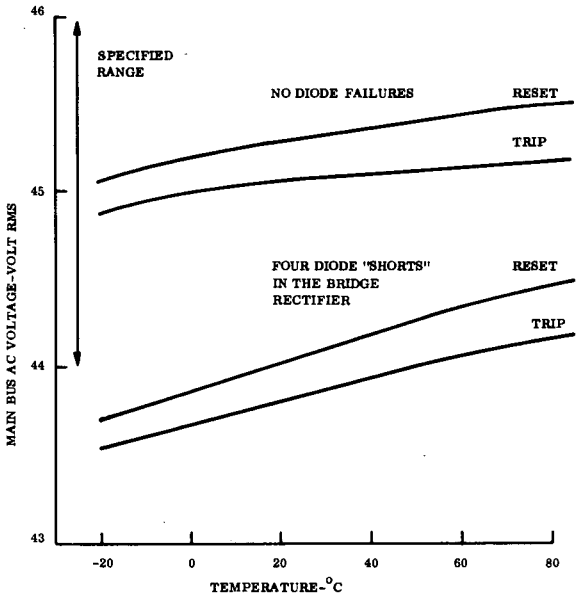


Figure 5.10-5. LVCO Qual Unit Trip Voltage

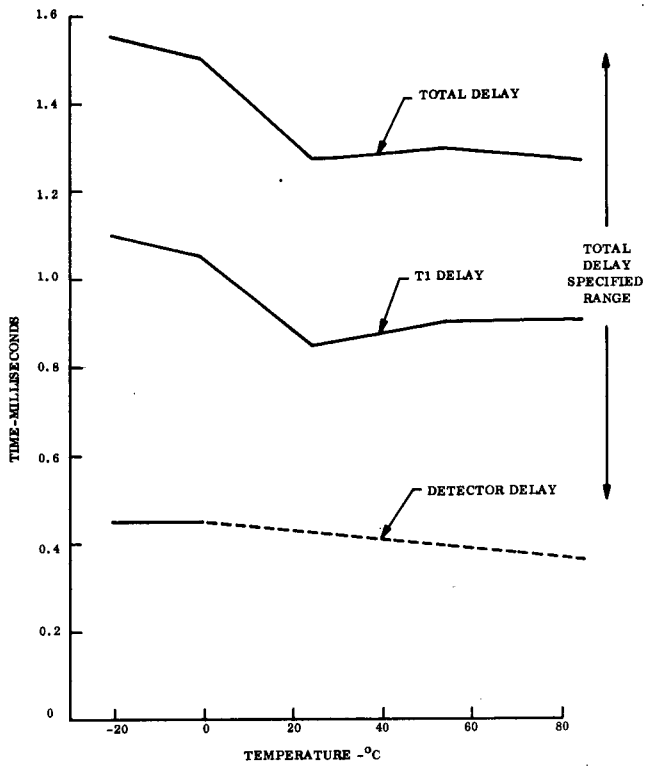


Figure 5.10-6. LVCO Qual Unit Detector Delay and T1 Delay

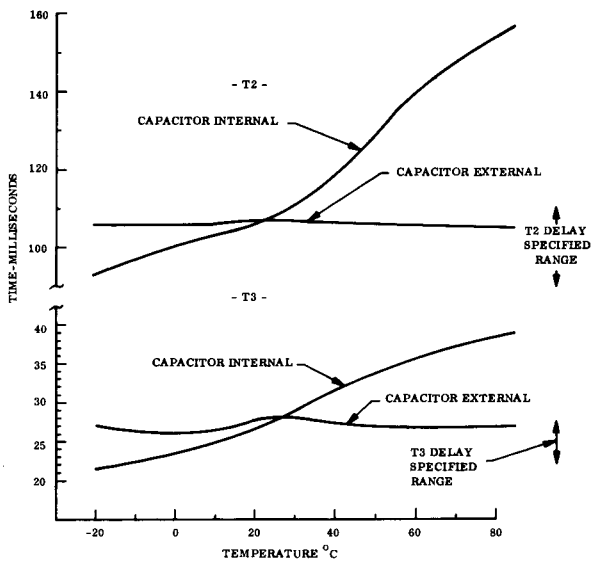


Figure 5.10-7. LVCO Qual Unit T2 Delay and T3 Delay

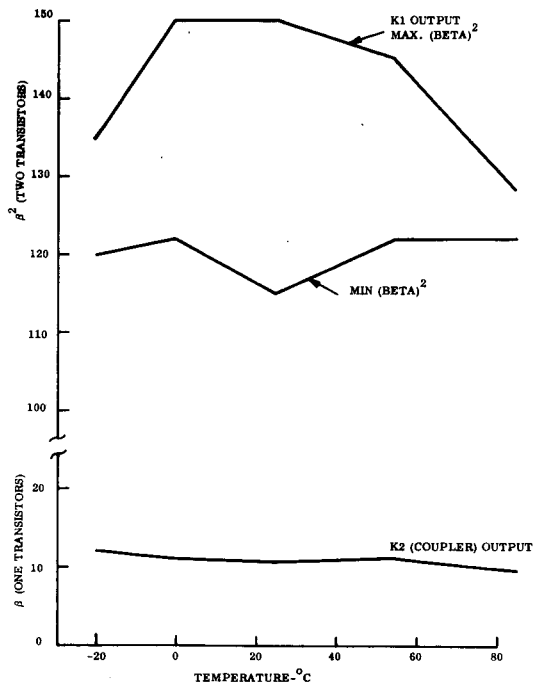


Figure 5.10-8. LVCO Qual Unit T3 Output Current

There is a small delay in the detector output due to the filter on the transformer-rectifier output. This delay is about 0.4 milliseconds, according to test results, when the input ac is switched off. This delay, and the T1 timing results, are presented in Figure 5.10-6. The total delay from the occurrence of an undervoltage to the CCS alert is really T1 plus the detector delay, for a step change from normal voltage to an undervoltage. For a slowly degrading ac voltage, there would be no detector delay.

Figure 5.10-7 presents the results for the second and third time out. The 29 F-type tantalum capacitor produced predictable variance with temperature. A temperature stable capacitor must be used to get the precise results currently specified. As demonstrated by the curves when the capacitor was not in the temperature chamber, there was little contribution to a change in timing from the other components in the timing circuit. These times are taken from photographs of oscilloscope traces thus the recording accuracy can be no better than ±0.5 millisecond for the T3 time. The variance of T3 timing was less than the allowed range, but it exceeded the range because the availability of specific resistors for trimming prevented setting the timing close to 25 milliseconds. The actual variation in T3 is too large a precentage of the allowable range to permit compliance with the spec over the full life of the mission. The accuracy problem is due to the fact that the timer hardware works from Tϕ (op amp output) while the spec is T0-T1, T1-T2, T2-T3. The timer tested cannot meet the referenced spec for the temperature range and life of the mission.

Figure 5.10-8 presents the current output results for T3 outputs. Since the actual current output has little meaning, the graph shows the amplification required by the device to produce its end result; i.e., transferring a relay. Since a relay is basically a current motivated device, the current required to operate a proposed relay (12 milliamp, 1/2 crystal can, 32 volt) was divided by the current provided by the LVCO output. For the K2 (coupler) transistor of the Power Distribution Switch, the collector current is 0.429 milliamp. The curves of Figure 5.10-8 include the results for the base-emitter shorted outputs as well as the no simulated failure results. More variation occurs in the K1 output because the small voltage changes

which occur cause larger current changes across the lower resistance. Due to the design of the switch, hard saturation is not required of the transistors in the switch, therefore a beta of 12 or even 15 could be acceptable, so the outputs for T3 meet the requirements.

The power consumed in standby mode is approximately 500 milliwatts. Approximately 100 milliwatts are losses in the transformer and the rest is in the sense resistor divider, series regulator reference, op amp and timing resistor ladder. Thus this design cannot meet the 100 milliwatt power dissipation requirement.

In general, the energy storage and coupling capacitors proved adequate. Likewise, the LVCO functioned correctly, providing sufficient output magnitude and duration in the test where the energy storage capacitors were not charged.

5.10.4 FAILURE MODE, EFFECT, AND CRITICALITY ANALYSIS

The Failure Mode, Effect, and Criticality Analysis (FMECA) performed on this component is shown on Table 5.10-1. Its purpose was to analyze the operation of each piece part to determine single failure effects on the component operation.

5.10.4.1 Piece Part Failure Effects

Since the philosophy of the LVCO is to provide an unsophisticated backup to fault correction of power problems, no extensive redundancy to perform the function is incorporated. Several key points such as rectification and filtering have quad's to prevent power overloading due to a single failure. The T/R and filtering is also the most "active" part of the circuit. A parallel power path must be provided for the noncritical load bus, but that is primarily as a backup to the K2 relay, not LVCO operation failures.

Whatever the LVCO can do (turn off, turn on, switch over) can occur erroneously or not occur when required, due to a single piece part failure. Erroneous outputs due to the detector and associated parts up to the FETs can be prevented by the inhibit command. An erroneous CCS interrupt output will just be ignored after the CCS confirms that no problem exists. An erroneous turnoff of noncritical loads can be corrected by CCS closing of K1. Erroneous

outputs to critical components on T3 are limited due to capacitive coupling, hence can occur only once.

Since this component only provides a backup function, failure to operate due to a single failure does not produce a single failure effect to the mission. Erroneous outputs can cause as little as one load to come on or go off, or as much as all critical loads switched to backup, due to a single failure. This is not to say there are many components which can fail to cause these drastic erroneous responses. There are only a few parts, and they must fail short, which can produce the large perturbations.

A relatively simple modification to the present LVCO design could prevent the erroneous single failure modes mentioned above. A series power switch, controlled by the op amp output, would apply voltage to a particular function output circuit only when an undervoltage is being detected. A possible method is schematically given in Figure 5.10-9. Two switches would be used, one each for T2 and T3.

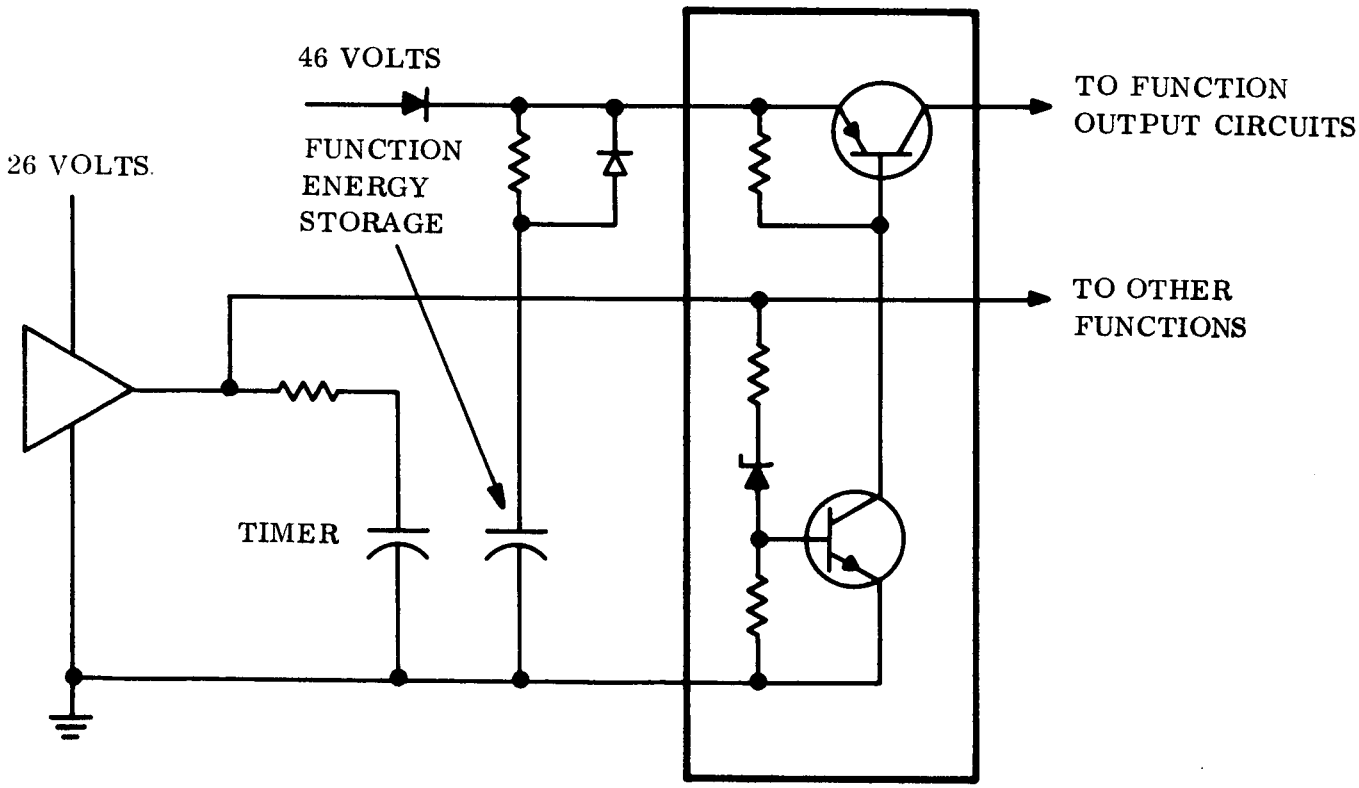


Figure 5.10-9. Series Switch Schematic - LVCO Modification

Another alternative, which is safer because it would provide inhibiting of the power switch by CCS inhibit, is given in Figure 5.10-10. While these additions reduce the probability of operation, the elimination of undesirable erroneous failure modes produces an LVCO even more consistent with its basic philosophy.

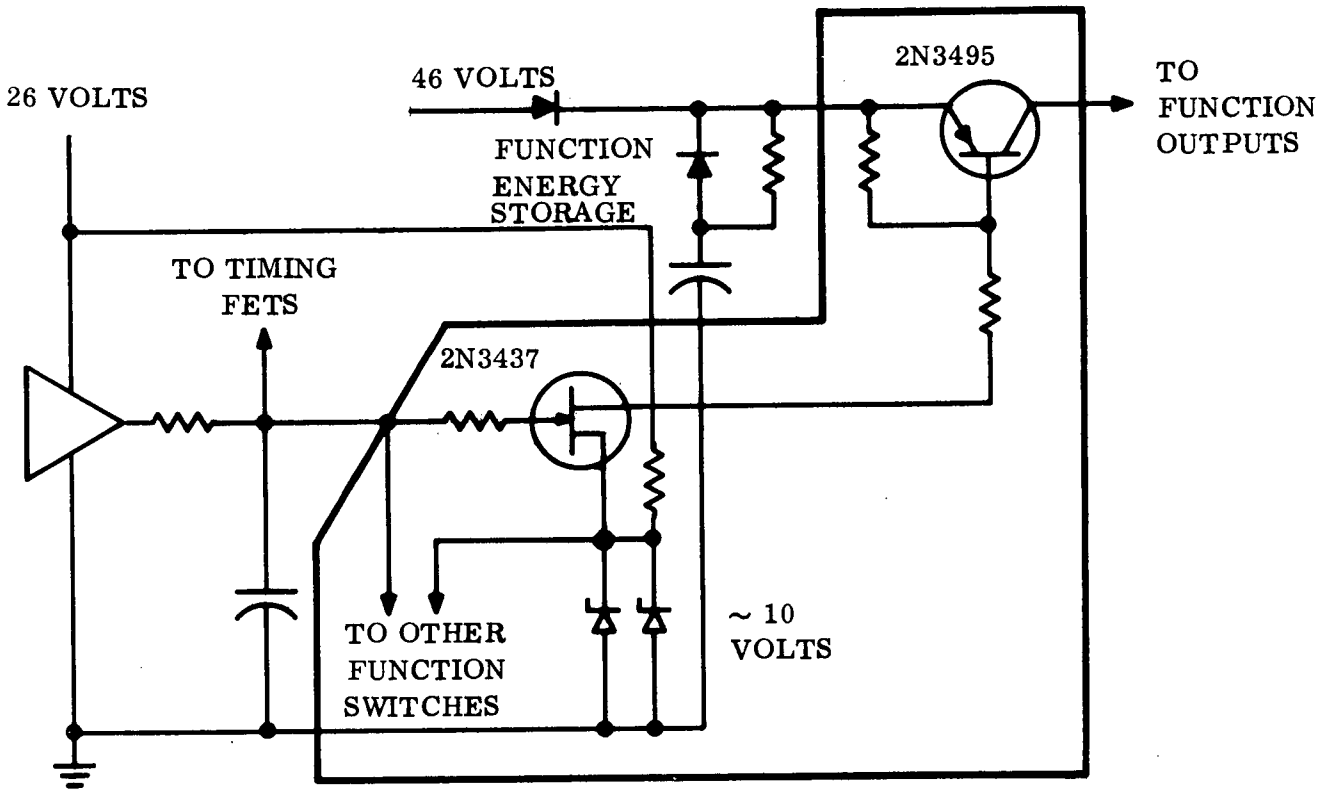


Figure 5.10-10. Series Switch Schematic - CCS Inhibited

The present design uses the 2N2222A transistor as the load switch driver. To provide for the possible 41 vdc transient undervoltage due to an open circuit failure of the Current Throttle, it is recommended that the 2N2222A transistor with a Vceo of 40 volts be replaced by a transistor with a Vceo of 60 volts or higher.

5.10.4.2 Circuit Failure Modes and Probability of Occurrence

The philosophy for LVCO use is that it is a simple hardware back-up to the CCS fault correction capability. As such, the circuit design has single failure modes that perturbate the spacecraft. The LVCO failures which affect system operation are summarized in Table 5.10-2.

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
1	R1	Resistor	Part of the voltage divider which samples the rectified AC Main Bus voltage.	Open		Inverting input to the A1 Op Amp goes low causing the output to go high.	Unless stopped by the LVCO inhibit command, the LVCO will perform all of its functions.	Failure is non-repetitive Loads can be restored to initial configuration by commands.	
2	R2	Resistor	Part of the voltage divider which samples the rectified AC Main Bus voltage.	Open		Inverting input to the A1 Op Amp goes high. Output will remain low.	NONE		LVCO can't perform its function It will remain inoperative.
3	R3	Resistor	Limits current to voltage reference diode CR13	Open		Non-inverting input to the A1 Op Amp goes low. Output will remain low.	NONE		LVCO can't perform its function It will remain inoperative.
4	R4	Resistor	Limits current to non-inverting input of A1 Op Amp	Open		Non-inverting input to the A1 Op Amp goes low. Output will remain low.	NONE		LVCO can't perform its function It will remain inoperative.
5	R5	Resistor	Feedback which provides hysteresis so that trip and reset voltage levels are not coincident.	Open		Oscillation of Op Amp output if input voltage was right at the trip point.	NONE		It is possible that the LVCO won't operate until the undervoltage condition became worse.
6	R6	Resistor	In conjunction with C3 & CR14 determines the delay of the CCS interrupt command.	Open		Loss of CCS interrupt command when the A1 Op Amp output goes high.	Can't inform CCS that the LVCO has detected an undervoltage condition on the Main Bus.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
7	R7	Resistor	Provides a path to ground for CR14 zener diode current	Open		CR14 won't conduct and turn off Q2 when A1 Op Amp goes high.	Loss of CCS interrupt command.		
8	R8	Resistor	Provide ground isolation between LVCO return and the CCS interrupt reference	Open		Probably none as the voltage applied to the Q2 gate is much higher than the pinch-off voltage required for this FET.	———		
9	R9	Resistor	Limits the charge current of energy storage capacitor C2	Open		C2 won't charge	None unless the Protected Bus has been lost and the Main Bus under-voltage is large.		
10	R10	Resistor	Limits the base current to voltage regulator Q1	Open		Q1 cuts-off. No voltage to the control circuits of the LVCO.	NONE		LVCO can't perform its function. It will remain inoperative.

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
11	R11	Resistor	Limits base current to transistor Q3 when Op Amp output goes high.	Open		Transistor Q4 will turn on as soon as C4 charges to 1.4 VDC. Q4 will short out timing capacitor C6.	The LVCO has detected a Main Bus undervoltage, but won't time out. No loads would be changed or removed from the Main Bus.		LVCO can't perform its function. It will remain inoperative.
12	R12	Resistor	Q3 leakage resistor	Open		Q3 could turn on if leakage current was high.	The LVCO can't be inhibited by CCS in the event of an erroneous Op Amp output.		
13	R13	Resistor	Discharge resistor for C4 capacitor	Open		Capacitor C4 can't discharge below 0.7 VDC.	Reduction in transient immunity on the CCS inhibit command line.		
14	R14	Resistor	Limits base current to transistor Q4 when Op Amp output goes high and inhibit command is given.	Open		Q4 won't latch up and stay on after the LVCO inhibit command stops.	Capacitor C6 will only be shorted out for the duration of the LVCO inhibit command. All LVCO outputs will occur after inhibit command stops.	Failure is non-repetitive Loads can be restored to initial configuration by command.	
15	R15	Resistor	Determines the charge rate of timing capacitor C6	Open		Capacitor won't charge when Op Amp output goes high.	The LVCO has detected a Main Bus undervoltage, but won't time out. No loads would be changed or removed from the Main Bus.		LVCO can't perform its function. It will remain inoperative.

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
16	R16	Resistor	Determines the discharge rate of timing capacitor C6 when the CCS inhibit command is given.	Open		C6 can't be discharged by the LVCO inhibit command.	The LVCO can't be inhibited by CCS in the event of an erroneous Op Amp output.		
17	R17	Resistor	Q4 leakage resistor	Open		Q4 could turn on if leakage current were high, timing capacitor C6 would be shorted out.	The LVCO has detected a Main Bus undervoltage, but won't time out. No load would be changed or removed from the Main Bus.		LVCO can't perform its function. It will remain inoperative.
18	R18	Resistor	Limits base current of Q4 from the LVCO inhibit command.	Open		Loss of inhibit capability	The LVCO can't be inhibited by CCS in the event of an erroneous Op Amp output.		
19	R19	Resistor	Limits gate current to FET Q5	Open		FET Q5 won't turn on when capacitor C6 charges up.	The critical redundand spacecraft loads won't be switched from Main to Standby.		
20	R20		Provides feedback from Q7 to Q5 to increase response time of Q5 - Q7 turn on.	Open		Won't have the snap action turn on of Q5 - Q7.	NONE		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
21	R21	Resistor	Forms a voltage divider network with which determines gate voltage at which Q5 & Q6 will be biased on.	Open		Divider network is open circuited.	The LVCO has detected a Main Bus undervoltage, but won't time out. No load would be changed or removed from the Main Bus.		LVCO can't perform its function. It will remain inoperative.
22	R22	Resistor	Limits base current to Q7.	Open		Q7 won't turn on when Op Amp output goes high.	The critical redundant spacecraft loads won't be switched from Main to Standby.		
23	R23	Resistor	Q7 leakage resistor	Open		Q7 could turn on if leakage current was high.	The critical redundant spacecraft loads would be switched from Main to Standby.	Failure is non-repetitive Loads can be restored to initial configuration by command.	Changes spacecraft loads.
24	R24	Resistor	Limits gate current to FET Q6	Open		FET Q6 won't turn on when capacitor C6 charges up.	The non-critical loads won't be switched off.		
25	R25	Resistor	Forms a voltage divider network with which determines gate voltage at which Q5 & Q6 will be biased on.	Open		Divider network is open circuited.	The LVCO has detected a Main Bus undervoltage, but won't time out. No load would be changed or removed from the Main Bus.		LVCO can't perform its function. It will remain inoperative.

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
26	R26	Resistor	Provides feedback from Q8 to Q6 to increase response time of Q6-Q8 turn on.	Open		Won't have the snap action turn on of Q6-Q8.	NONE		
27	R27	Resistor	Forms a voltage divider network with which determines gate voltage at which Q5 & Q6 will be biased on.	Open		Divider network is open circuited.	The LVCO has detected a Main Bus undervoltage, but won't time out. No load would be changed or removed from the Main Bus.		The LVCO can't perform its function. It will remain inoperative
28	R28	Resistor	Limits the base current to Q8	Open		Q8 won't turn on when Op Amp output goes high.	The noncritical loads won't be switched off.		
29	R29	Resistor	Q8 leakage resistor	Open		Q8 could turn on if leakage current was high.	The non-critical loads would be switched off.	These loads can be turned back on by the LVCO bypass command	Changes spacecraft loads.
30	R30	Resistor	Limits charge rate of energy storage capacitor C7	Open		Capacitor C7 can't be charged.	None unless the Protected Bus has been lost and the Main Bus undervoltage is large.		
31	R31	Resistor	UNDETERMINED						

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
32	R32	Resistor	Limits base current to Q9	Open		Q9 won't turn on when commanded by Q8	The non-critical loads won't be switched off.		
33	R33	Resistor	Q10 leakage resistor	Open		Q10 could turn on if leakage current was high.	The non-critical loads would be switched off.	These loads can be turned back on by the LVCO by-pass command.	Changes space-craft loads.
34	R34	Resistor	Limits the base current of Q10	Open		Q10 won't turn on when commanded by Q9.	The non-critical loads won't be switched off.		
35	R35	Resistor	Q9 leakage resistor	Open		Q9 could turn on if leakage current was high.	The non-critical loads would be switched off.	These loads can be turned back on by the LVCO by-pass command.	Changes space-craft loads.
36	R36	Resistor	Limits base current of Q9 from the CCS command "Non-critical loads off".	Open		Q9 won't turn on when commanded by CCS.	Can't turn the non-critical loads off by this single command.		
37	R37	Resistor	Q11 leakage resistor	Open		Q11 could turn on if leakage current was high.	The K2 close coil would remain activaced preventing the control circuits from turning off non-critical loads.		
38	R38	Resistor	Limits base current of Q11	Open		Q11 won't turn on when commanded by Q12. Can't reset the K2 relay after the LVCO has turned off the non-critical loads.	The LVCO could not turn off the non-critical loads in any future operation.		The LVCO bypass command must be given in order to turn the non-critical loads back on.

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
39	R39	Resistor	Q12 leakage resistor	Open		Q12 could turn on if leakage current was high.	The K2 close coil would remain activated preventing the control circuits from turning off non-critical loads.		
40	R40	Resistor	Limits base current of Q12 from the CCS command "LVCO Reset".	Open		Can't close the K2 relay after the LVCO has turned off the non-critical loads.	The LVCO could not turn off the non-critical loads in any future operation.		The LVCO bypass command must be given in order to turn the non-critical loads back on.
41	R41	Resistor	Q14 leakage resistor	Open		Q14 could turn on if leakage current was high. K1 open relay coil would remain activated.	The LVCO could not be bypassed if required.		
42	R42	Resistor	Limits base current of Q14	Open		Q14 won't turn on when commanded by Q13. Can't open the LVCO bypass relay.	The LVCO could not turn off the non-critical loads in any future operation.		
43	R43	Resistor	Q13 leakage resistor	Open		Q13 could turn on if leakage current was high. K1 open relay coil would remain activated.	The LVCO could not be bypassed if required.		
44	R44	Resistor	Limits base current of Q13 from the CCS command "LVCO Reset".	Open		Can't open the K1 relay after the LVCO bypass command has been given.	The LVCO could not turn off the non-critical loads in any future operation.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
45	R45	Resistor	Q16 leakage resistor	Open		Q16 could turn on if leakage current was high. K1 close relay coil would remain activated.	The LVCO could not turn off the non-critical loads in any future operation.		
46	R46	Resistor	Limits base current of Q16.	Open		Q16 won't turn on when commanded by Q15. Can't bypass the LVCO.	NONE		If this function was required, there must first be a failure in the K2 section of the LVCO which prevents closing the K2 relay. The failure of the LVCO bypass constitutes the second failure.
47	R47	Resistor	Q15 leakage resistor	Open		Q15 could turn on if leakage current was high. K1 close relay coil would remain activated.	The LVCO could not turn off the non-critical loads in any future operation.		
48	R48	Resistor	Limits base current of Q15 from the CCS command "LVCO Bypass".	Open		Can't close the K1 relay.	NONE		If this function was required, there must first be a failure in the K2 section of the LVCO which prevents closing the K2 relay. The failure of the LVCO bypass constitutes the second failure.
49	R49	Resistor	Limits the current thru FET Q17.	Open		Q17 won't turn on Q18 when voltage is applied to point "A"	The critical redundant loads can't be switched from prime to back-up.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
50	R50	Resistor	In conjunction with capacitor C8, determines the time that Q17 remains on.	Open		Q17 won't turn off.	NONE		Q17 timing circuit was introduced because if concern that leakage current might prematurely activate a power distribution switch at a critical redundant load.
51	R51	Resistor	Limits gate current of FET Q17.	Open		Q17 won't turn off.	NONE		
52	R52	Resistor	Q18 leakage resistor	Open		Q18 would turn on if leakage current was high.	All critical redundant loads would be switched from main to stand by.	Failure is non-repetitive. Loads can be restored to initial configuration by command.	The switching of critical redundant loads could not be performed by the LVCO in any subsequent operation changes spacecraft loads.
53	R53	Resistor	Limits charge rate of energy storage capacitor C10.	Open		Capacitor C10 can't be charged.	None unless the Protected Bus has been lost and the Main Bus undervoltage is large.		
54	R54	Resistor	Discharge resistor for capacitor C9	Open		Capacitor C9 can't discharge when Q18 turns off.	NONE		The switching of critical redundant loads could not be performed by the LVCO in any subsequent operation.

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
55	R55	Resistor	Q19 leakage resistor	Open		Q19 could turn on if leakage current was high.	One critical redundant load will change state. As a result, two like items could be on together, or both like items could be off, or one item could turn on when that function is not required.		Changes space-craft loads.
56	R56	Resistor	Discharge resistor for capacitor C11	Open		Capacitor C11 can't discharge when Q19 turns off.	The load controlled by Q19 won't be switched in sub-sequent operations of the LVCO.		
57	R57	Resistor	Limits output current to the power distri-bution switch	Open		Command to the power distribution switch is open circuited.	None as each power distribution switch has two commands from the LVCO.		
58	CR 1	Diode Quad	In conjunc-tion with CR2 thru CR4, full wave rectify the Main AC Bus voltage to provide a DC measurement of the voltage magnitude.	Open or Short		A failure short will increase the rectified voltage slightly.	The bus voltage would have to go slightly lower before the LVCO would trip.		No serious failure effects as the diode is series - parallel redundant. (quad.)
	NOTE:	Diode quads and effects	CR 2 thru CR 4 as CR 1 above	have the same failure modes					

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
59	CR5	Diode Quad	Provides isolation of the Main Bus from under-voltage on the Protected Bus.	Open or Short		NONE	NONE		No serious failure effects as the diode is series - parallel redundant (quad.)
60	CR7	Diode Quad	Provides isolation of the Protected Bus from under voltage on the Main Bus.	Open or Short		NONE	NONE		No serious failure effects as the diode is series - parallel redundant (quad)
	NOTE:	Diode quad CR 6 has the same failure modes and effects as CR 5 Diode quad CR 8 has the same failure modes and effects as CR 7							
61	CR9	Diode	Prevents energy storage capacitor C2 from discharging into the Main Bus voltage sense resistor divider network.	Open		NONE	NONE	Diode is parallel redundant.	If not parallel redundant, an open would prevent charging of C2 hence loss of LVCO control circuitry.
				Short		C2 would discharge into R1 - R2.	None - capacitor would discharge slightly faster.		
62	CR10	Zener Diode	Provides a reference for the voltage regulating transistor Q1.	Open		Q1 would remain full on. Loss of voltage regulation. Terminal voltage on all circuits would be approx. 47 VDC. Op Amp A-1 would fail.	LVCO would not operate.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
62				Short		Q1 would turn off. No voltage to control circuits.			
63	CR11	Diode	Provides discharge path for energy storage capacitor C2.	Open		Discharge thru R9 would not provide adequate voltage to operate the control ckts. Ckts. can operate from the Protected Bus.	LVCO would not operate if the Protected Bus has been previously lost.		
				Short		Charging current into C2 would be excessive. Could fail capacitor.	If capacitor fails short, it will short circuit both DC buses.		
64	CR12	Diode	Compensates for the variation in voltage drop of the diodes in the full wave rectifier due to temperature changes.	Open		Inverting input to A1 Op Amp goes high keeping the output low.	LVCO won't operate unless the Main Bus voltage goes very low. (less than 10 VDC)		
				Short		Input voltage at the inverting input to A1. Op Amp would drop. Could cause the output to go high.	LVCO would operate prematurely.	Can be stopped by the LVCO inhibit command.	
65	CR13	Zener Diode	Voltage reference for A1 Op Amp	Open		Non-inverting input to A1 Op Amp goes high output will go high.	LVCO would operate prematurely.	Can be stopped by the LVCO inhibit command.	

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
65				Short		Non-inverting input to A1 Op Amp goes low causing the output to remain low.	LVCO would not operate.		
66	CR14	Zener Diode	Minimum Op Amp output voltage would cause pinch off of FET Q2. This zener voltage drop prevents this.	Open		Q2 could not be turned off when Op Amp output goes high.	CCS interrupt signal would be lost.		
				Short		Q2 would be turned off prematurely.	Erroneous CCS interrupt signal would be issued.		
67	CR15	Diode	In conjunction with CR16 provides sufficient voltage drop when Q4 turns on that base drive to Q3 is removed and Q3 turns off.	Open		Q3 doesn't turn on. Q4 does turn on and prevents timing capacitor C6 from charging.	LVCO would not operate.		
				Short		If Q4 is commanded on, the voltage drops might not be adequate to remove base drive from Q3. When command is removed, Q4 would shut off.	NONE		LVCO inhibit circuit would not work. Couldn't stop a failed LVCO from switching the spacecraft loads.
	NOTE:	Diode CR16 has the same failure modes and effects as CR15							

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
68	CR17	Zener Diode	Minimum Op Amp output voltage would cause turn on of Q4. This zener voltage drop prevents this.	Open		Q4 would drop out after the LVCO inhibit command stopped. Latchup circuit wouldn't work.			LVCO inhibit circuit would not work. Couldn't stop a failed LVCO from switching the spacecraft loads.
				Short		Q4 would always be on, even when Op Amp output is low. If Op Amp went high, timing capacitor C6 would remain shorted.	LVCO would not operate.		
69	CR18	Diode	Isolates the LVCO inhibit command and prevents charging capacitor C4.	Open		Q4 would drop out after the LVCO inhibit command stopped. Latchup circuit wouldn't work.			LVCO inhibit circuit would not work. Couldn't stop a failed LVCO from switching the spacecraft loads.
				Short		LVCO inhibit command would be grounded by Q3. Q4 wouldn't turn on.			LVCO inhit circuit would not work. Couldn't stop a failed LVCO from switching the spacecraft loads.
70	CR19	Diode	Provides a fast discharge for timing capacitor C6 when the Op Amp output goes low.	Open		C6 won't discharge rapidly when Op Amp output goes low. If Op Amp went high shortly after going low, the intitial voltage on the capacitor would be high and hence would shorten the time delay of the LVCO outputs.	LVCO could time out faster than planned. This would shorten the time allotted to CCS to correct the undervoltage problem.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
70				Short		Limiting resistor R15 is shorted. Capacitor C6 charges too quickly.	All LVCO events occur prematurely CCS doesn't have time to correct the Main Bus voltage problem.		
71	CR20	Diode	Prevents the anode of CR16 from being only one diode drop above ground at turn on and thus preventing Q3 turn on.	Open		If Q4 were commanded on (LVCO inhibit), the capacitor C6 could not be shorted.			LVCO inhibit circuit would not work. Couldn't stop a failed LVCO from switching the spacecraft loads.
				Short		NONE	NONE	Diode is series redundant.	
72	CR21	Diode Quad	Provides a redundant power path from the 30 VDC buses to operate the K2 open relay coil while also preventing the capacitor C7 from discharging into these DC buses.	Open or Short		NONE	NONE		No serious failure effects as the diode is series - parallel redundant (quad)

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
73	CR22	Diode	Provides isolation to prevent the DC buses from grounding in the event of a shorted C7 capacitor.	Open		Energy storage capacitor C7 won't discharge into K2 open relay coil.	None - energy storage backed up by the DC buses.		
				Short		None unless capacitor C7 shorts	NONE		
74	CR23	Diode	Prevents capacitor C7 from discharging into the 48 V bus when the bus voltage goes low.	Open		Energy storage capacitor C7 won't charge.	None unless both DC buses go low, then the non-critical loads can't be turned off by the LVCO.		
				Short		C7 will discharge into the 48 VDC bus when the AC Main Bus goes low.			
75	CR24	Diode	Provides isolation for the CCS command "N.C. loads off" in the event of a low in the LVCO circuitry	Open		Can't operate the K2 open relay coil by the LVCO control circuitry.	Non-critical loads can't be turned off by the LVCO.		
				Short		None unless the LVCO control circuitry fails low.	NONE		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
76	CR25	Diode	Provides isolation for the LVCO command "N.C. Loads Off" in the event of a low in the CCS command circuitry.	Open		Can't operate the K2 open relay coil by the CCS command circuitry.	Non critical loads can't be turned off by the LVCO.		
				Short		None unless the CCS command circuitry fails low.	NONE		
77	CR26	Diode	Relay coil transient suppression	Open		Current spike on DC line when Q10 shuts off.	Could cause interference with other circuits.		
				Short		K2 open coil could not be energized.	Non-critical loads can't be turned off by the LVCO.		
78	CR27	Diode	Relay coil transient suppression	Open		Current spike on DC line when Q11 shuts off.	Could cause interference with other curcuits.		
				Short		K2 close coil could not be energized.	Non-critical loads can't be turned back on and this function can't be reset. Next LVCO operation won't turn off the non-critical loads.	Non-critical loads can be turned on by the LVCO bypass (K1 close) command.	

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
79	CR28	Diode	Prevents reverse bias on Q12 base-emitter in the event that the CCS command goes negative.	Open		K2 close coil could not be energized.	Non-critical loads can't be turned back on and this function can't be reset. Next LVCO operation won't turn off the non-critical loads.	Non-critical loads can be turned on by the LVCO by pass (K1 close) command.	
				Short		None unless the command goes negative	NONE		
	NOTE:	Diodes CR29 and CR31 perform the same function for relay K1 as diodes CR26 and CR27 perform for relay K2.							
	NOTE:	Diodes CR30 and CR32 perform the same function for their respective transistors as diode CR28 does for Q12.							
80	CR33	Diode	In conjunction with CR34 provides forward bias voltage required to turn on the transistors required to switch critical loads.	Open		The forward bias voltage would be higher, causing the coupling capacitors (EX. C11) to charge faster. Hence, the duration of the command to the power distribution switch would be shortened.	The command duration is reduced from about 19 milliseconds to about 12 milliseconds. The power distribution switches will probably still work.		CR33 consists of four series diodes. The failure effects described are the result of one of the four failing.
				Short		The forward bias voltage would be decreased. Command duration would increase but command current would be smaller.	None - The power distribution switches would probably still work.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
81	CR34	Zener Diode	In conjunction with CR33 provides forward bias voltage required to turn on the transistors required to switch critical loads.	Open		The forward bias voltage would be higher, causing the coupling capacitors (EX. C11) to charge faster. Hence, the duration of the command to the power distribution switch would be shortened.	The command duration is reduced from about 19 milliseconds to about 12 milliseconds. The power distribution switches will probably still work.		
				Short		Voltage would not be adequate to turn on the downstream transistors.	The LVCO can't switch the critical redundant loads.		
82	CR35	Diode	Provides isolation such that the energy storage capacitor C10 doesn't discharge into the 48 V bus during an undervoltage.	Open		C10 can't charge. No power available for this circuit.	LVCO can't switch the critical redundant loads.		
				Short		None unless both DC buses are low during the undervoltage condition.	If both buses are low, LVCO can't switch the critical redundant loads.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
83	CR36	Diode	Provides low impedance discharge path for C10 into control circuits.	Open		Discharge thru R53 would not provide adequate voltage to operate the control circuits. If the Protected Bus is good, this circuit will operate from it.	LVCO can't switch the critical redundant loads if the Protected Bus has been previously lost.		
				Short		Charging current into C10 would be excessive. Could fail capacitor.	If the capacitor fails short, it will short circuit both DC buses.		
84	CR37	Diode	Prevents a collector to base short of Q19 from turning on the other four command transistors.	Open		Q19 can't be turned on when commanded.	When the LVCO commands the critical loads to switch, one load won't respond.		
				Short		None unless Q19 shorts collector to base.	NONE		
85	CR38	Diode	Provides isolation at the command input to the power distribution switch in the event of a failure of Q19 short emitter to base.	Open		Output to one section of the power distribution switch is lost.	NONE	Each power distribution switch has two command outputs from the LVCO.	
				Short		None unless Q19 fails short emitter to base.	NONE		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
86	C1	Capacitor	Filters the rectified AC Main Bus input.	Open		Capacitance will be reduced by half.	NONE	Capacitor is quad redundant	C1 consists of four capacitors. The failure effects described are the result of one of the four failing.
				Short		Capacitance will be increased. Will slightly decrease the response of the LVCO to an undervoltage condition.	NONE		
87	C2	Capacitor	Provides energy storage for the LVCO control and timing ckts. in the event that both DC buses go low.	Open or Short		None unless both DC buses are low at the time of a Main Bus under-voltage.	NONE		
88	C3	Capacitor	In conjunction with R6 determines the timing of the CCS interrupt to the computer.	Open		Q2 will be pinched off as soon as the Op Amp output goes high.	CCS interrupt would be given prematurely, Op Amp output could have gone high due to a transient on the Main Bus.		The purpose of this time delay before the CCS interrupt is given is to provide transient immunity.
				Short		Q2 won't be pinched off. Q2 gate would be grounded.	CCS would not be informed that the LVCO has sensed a failure.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
89	C4	Capacitor	Provides a delay so that Q3 can turn on and prevent Q4 turn on when the Op Amp output goes high.	Open		A race condition exists between Q3 and Q4 when Op Amp goes high. Which even turns on first prevents the other from turning on.	The LVCO would be inhibited if Q4 is first to turn on.		
				Short		Q4 would not latch-up after the LVCO inhibit command dropped out.	The LVCO can't be inhibited.		
90	C5	Capacitor	AC couples the LVCO inhibit command to prevent a failure high of the command source from inhibiting the LVCO.	Open		LVCO inhibit command won't be received by Q4	LVCO can't be inhibited.		
				Short		None unless the command source fails high.	NONE		
91	C6	Capacitor	Provides the timing of the LVCO outputs.	Open		All FETS are immediately turned on when the Op Amp output goes high.	All LVCO outputs occur immediately and simultaneously when the under-voltage failure is detected.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
91				Short		All FET gates are grounded.	The LVCO would not perform any corrective functions. No loads would be switched by the LVCO.		
92	C7	Capacitor	Provides energy storage for the non-critical loads off function.	Open or Short		None unless both DC bases are low at the time of the Main Bus under voltage.	NONE		
93	C8	Capacitor	In conjunction with R50, determines the duration of the signal to the switch critical load command	Open		Q17 would be turned off as soon as the signal from the timing circuit went high.	The switch critical load function would not work.		
				Short		Q17 would not turn off.	Current from the timing circuit could keep some of the power distribution switches energized.		
94	C9	Capacitor	Determines the duration of the Q18 collector current into the command generation transistors	Open		Base drive to the command generator transistors is lost.	The switch critical load function would not work.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
94				Short		Q18 collector current would continue until base drive is removed by Q17.	NONE		
95	C10	Capacitor	Provides energy storage for the LVCO "switch critical loads" function in the event that both DC buses go low.	Open or Short		None unless both DC buses are low at the time of a Main Bus under-voltage.	NONE		
96	C11	Capacitor	AC couples the command generation transistor Q19 to the power distribution switch so that a Q19 short won't keep the switch energized.	Open		Q19 can't be turned on when commanded	When the LVCO commands the critical loads to switch, one load won't respond		
				Short		None unless Q19 fails short	NONE		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
97	T1	Transformer	Provides a sample of the AC Main Bus voltage.	Open or Short Secondary		The inverting input of the Op Amp goes low causing the output to go high.	LVCO starts its operations	Can be inhibited by CCS.	
				Short Primary		Secondary voltage goes high.	LVCO won't detect a undervoltage on the AC bus.		
98	A1	Operational Amplifier	Compares the sampled AC voltage with a reference to detect an undervoltage condition.	Output High		All circuits begin operation	LVCO will charge the state of the spacecraft loads	Can be inhibited by CCS.	
				Ouput Low		NONE	The LVCO won't detect or correct an undervoltage on the AC Bus.		
99	Q1	Transistor	In conjunction with CR10, regulates the output voltage to 26 VDC	Open		The control circuits are inoperative.	The LVCO won't detect or correct an undervoltage on the AC Bus		
				Short		Op Amp voltage is too high. Could cause failure.			
100	Q2	FET Transistor	Provides the CCS interrupt signal to inform the computer that the LVCO is going to change the state of the loads.	Open or Short		Q2 can't be pinched off to provide a high source to drain impedance.	No CCS interrupt signal is transmitted.		

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
101	Q3	Transistor	Keeps Q4 LVCO inhibit transistor from turning on unless commanded by CCS.	Open		Q4 will turn on when Op Amp output goes high and will short out the timing capacitor C6.	The LVCO would be inhibited.		
				Short		Q4 won't latch-up after the LVCO inhibit command drops out.	The LVCO can't be inhibited.		
102	Q4	Transistor	Inhibits the LVCO in the event that a internal failure has caused it to begin operation.	Open		Q4 can't short the timing capacitor C6	The LVCO can't be inhibited.		
				Short		The timing capacitor C6 would always be shorted.	The LVCO won't operate to clear the Main Bus fault.		
103	Q5	FET Transistor	Turns on the "Switch Critical Loads" function when the proper voltage builds up on C6.	Open		Q7 can't be turned on.	The "Switch Critical Loads" function won't occur		Changes spacecraft loads.
				Short		Q7 will be turned on as soon as the short on Q5 happen	The "Switch Critical Loads" will be performed at this time.	This failure is non-repetitive as the outputs are AC coupled.	

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
104	Q6	FET Transistor	Turns on the "Non-critical Loads Off" function when the proper voltage builds up on C6.	Open		Q8 can't be turned on.	The "Non-critical Loads Off" functio won't occur.		Suggest that this "Non-critical Loads Off" funtion be AC coupled so that the relay coil does not remain energized when a piece part fails.
				Short		Q8 will be turned on as soon as the short on Q6 happen	The "Non-critical Loads Off" will be performed at this time.		Changes space-craft loads.
105	Q7	Transistor	Amplifies the Q5 signal	Open		Q18 can't be turned on	The "Switch Criti-cal Loads" functio won't occur.		Changes space-craft loads.
				Short		Q18 will be turned on as soon as the short on Q7 happens.	The "Switch Criti-cal Loads" will be performed at this time.	This failure is non-repet-tive as the outputs are AC coupled.	
106	Q8	Transistor	Amplifies the Q6 signal	Open		Q9 can't be turned on.	The "Non-critical Loads Off" functio won't occur.		Suggest that this "Non-critical Loads Off" function be AC coupled so that the relay coil does not remain energized when a piece part fails.
				Short		Q9 will be turned on as soon as the short on Q8 happens	The "Non-critical Loads Off" will be performed at this time.		Changes space-craft loads.

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
107	Q9	Transistor	Amplifies either the LVCO command or the CCS command to turn off the non-critical loads.	Open		Q10 can't be turned on.	The "Non-critical Loads Off" function won't occur.		Suggest that this "Non-critical Loads Off" function be AC coupled so that the relay coil does not remain energized when a piece part fails.
				Short		Q10 will be turned on as soon as the short on Q 9 happens.	The "Non-critical Loads Off" will be performed at this time.		Changes space-craft loads.
108	Q10	Transistor	Amplifies the Q9 signal to turn off the non-critical loads.	Open		Relay K2 open coil can't be turned on.	The "Non-critical Loads Off" function won't occur.		Suggest that this "Non-critical Loads Off" function be AC coupled so that the relay coil does not remain energized when a piece part fails.
				Short		Relay K2 open coil will be turned on as soon as the short on Q10 happens.	The "Non-critical Loads Off" will be performed at this time.		Changes space-craft loads.
	NOTE:	Transistors Q12, Q13, Q15 and Q11, Q14, Q16 have the same failure modes as Q9 and Q10 respectively. Their failures effect their respective relay coils and their functions just as Q9 and Q10 do to K2 open relay coil.							

Table 5.10-1. Failure Mode, Effect, and Criticality Analysis (Cont'd)

Subsystem POWER
Component LVCO
Drawing No.

Prepared by R. Andrews

Item	Circuit Symbol	Part Type	Function	Failure Mode	Most Probable Cause of Failure	Failure Effect on Component	Failure Effect on Subsystem or System	Compensating Provisions	Remarks and Recommendations
109	Q17	FET Transistor	In conjunction with C8, limits the duration of the "Switch Critical Loads" command	Open		Q18 can't be turned on.	The "Switch Critical Loads" function won't occur.		
				Short		Q18 base drive will continue	NONE	Q18 collector is AC coupled to the command generation transistor.	
110	Q18	Transistor	Amplify the Q7 signal to switch critical loads.	Open		The command generation transistors can't be turned on.	The "Switch Critical Loads" function won't occur.		
				Short		The command generation transistors will be turned on as soon as the short on Q18 happens	The "Switch Critical Loads" will be performed at this time.	This failure is non-repetitive as the ouputs are AC coupled.	Changes spacecraft loads
111	Q19	Transistor	Amplify the Q18 signal and provide a command to a power distribution switch.	Open		The output to one power distribution switch is lost.	One critical load won't change state		
				Short		The output to one power distribution switch occurs at the time Q19 shorts	One critical load changes state prematurely.		Changes spacecraft loads

Table 5.10-2. LVCO Failure Summary

	Failure Mode		
Nature of Failure	CCS interrupt signal is issued without a bus voltage problem.	All noncritical loads turn off.	All critical loads are switched from main to standby units, or just one main load is switched off or one standby switched on.
Impact on Spacecraft	CCS must stop what it is doing and verify from other voltage monitors that the bus voltage is good.	Only critical loads remain in operation.	Temporary loss of Attitude Control until standby Cruise Sun Sensor and Canopus Sensor acquire their targets. Temporary loss of up link communication. Temporary loss of Command Decoder command capability. If only one load is effected, any one of the previous anomalies could occur.
Method of Correction	CCS issues an inhibit command to the LVCO.	CCS issues an override command which by-passes the LVCO and turns all loads back on.	CCS issues commands to return the critical loads to their original state.
Probability of Occurrence	Probability of erroneous interrupt signal NOT happening is 0.9792.	One of 3 transistors or 1 FET all of which are supporting voltage must fail short circuit. The probability of this NOT happening is 0.999.	One of 2 transistors or 1 FET all supporting voltage must fail short circuit for all critical loads to switch from main to standby. The probability of this NOT happening is 0.99925. The probability of any of the twenty critical loads NOT being turned on or off is 0.995. The probability of one specific load NOT being turned on or off is 0.99975.
Other Power Subsystem Failures which Cause the Same Effect	Failure of a voltage sensor would cause MPS to alert CCS.	It isn't obvious that a single failure of other hardware within the Power Subsystem could turn off all noncritical loads, but a single failure in the remote decoder or power distribution switch can turn off one noncritical load.	It isn't obvious that a single failure of other hardware within the Power Subsystem could turn all critical loads to their standby units, but a single failure in the remote decoder or power distribution switch can turn on or off one critical load.

(Note - All LVCO failures are nonrepetitive)

SECTION 6
TECHNOLOGY DEVELOPMENT

The following sections report on the status of technology developments undertaken during the program. These developments concern circuit designs for dedicated power conditioning elements not included in the Power Subsystem. These designs were breadboarded, tested and delivered to JPL. Together with the system definition activity, the results of the technology development effort will serve to define realistic PCE hardware requirements and capabilities.

6.1 TWT CONVERTER ASSEMBLY

6.1.1 FUNCTIONAL CHARACTERISTICS

1. Provides dc to dc conversion of electrical power to satisfy traveling wave tube requirements.

2. Input voltage: 30 vdc $\pm$ 1%

3. Output voltage:

   Helix: 3400 to 3500 vdc, setable within 0.2%; regulation $\pm$ 0.5%; ripple 1.0 volt peak to peak.

   Collector: 1425 to 1525 vdc, setable within 0.5%; regulation $\pm$ 1.0%; ripple 2.0 volts peak to peak.

   Anode: 100 to 500 vdc, setable within 5.0 volts; regulation $\pm$ 1%; ripple 1.0 volt peak to peak.

   Filament: 5.0 to 5.5 volts rms, setable within 0.1 volts; regulation $\pm$ 3%.

4. Current:

   Helix: 2 to 5 milliamperes

   Collector: 43 to 48 milliamperes

Anode: 0.2 milliamperes

Filament: 220 milliamperes with a 400 milliampere limit

5. Operation required through pressure decrease from atmosphere to space vacuum.

6.1.2 DESIGN DEFINITION

6.1.2.1 General Description

The Traveling Wave Tube Amplifier Power Supply provides power to the TWT as shown in Figure 6.1-1.

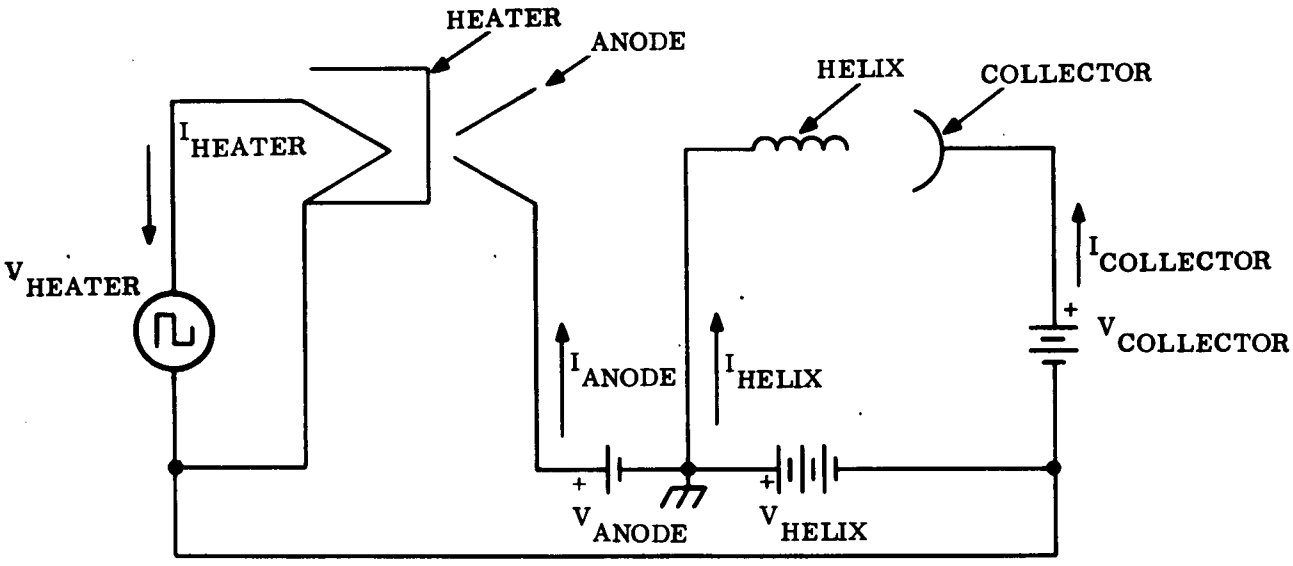


Figure 6.1-1. Traveling Wave Tube Amplifier Power Supply

The requirements for the particular voltages and currents are shown in Table 6.1-1.

Table 6.1-1. Requirements of the TWT DC-to-DC Converter

Output	Voltage	Current	Regulation	Ripple	Remarks
Heater	5.0 to 5.5 vrms	0.2 amps	$\pm$ 3.0%		Current Limited to 0.4 amps rms
Helix	3400 to 3500 vdc	2.0 to 5.0 ma	$\pm$ 0.5%	$<1.0\ V_{pp}$	Adjustable
Collector	1425 to 1525 vdc	43.0 to 48.0 ma	$\pm$ 1.0%	$<2.0\ V_{pp}$	Adjustable
Anode	100 to 400 vdc	0.2 ma	$\pm$ 1.0%	$<1.0\ V_{pp}$	Adjustable

- Provide heater voltage 110 seconds nominal prior to main power turn on.
- Turn TWT off below 29.4 volts and above 30.6 volts and inhibit the turn on of the main power if the input bus voltage is not in the 30 v $\pm$ 2% range.
- Switch from an input clock frequency of 8.192 kHz.

  Heater 4.096 kHz
  Main Power 2.048 kHz

- Free run if there is no clock input

The block diagram of the TWT Power Supply is shown in Figure 6.1-2. The heater and the high voltage converter (Figures 6.1-3 and 6.1-4) both utilize the same input filter, the heater supply turns on instantaneously upon input power application, and the high voltage outputs turn on 110 seconds later. Both the heater and the high voltage converters switch at the vehicle clock frequency of 4.096 kHz and 2.048 kHz respectively. They are also capable of switching at their own free running frequencies when the vehicle clock is absent.

The heater inverter utilizes a high reactance transformer to provide the desired output voltage and also provides current limiting as explained in the Heater Transformer section of this report. The high voltage converter is protected from over voltage and under voltage by a high and low voltage cutoff circuit shown in Figure 6.1-5. When in operation, the high

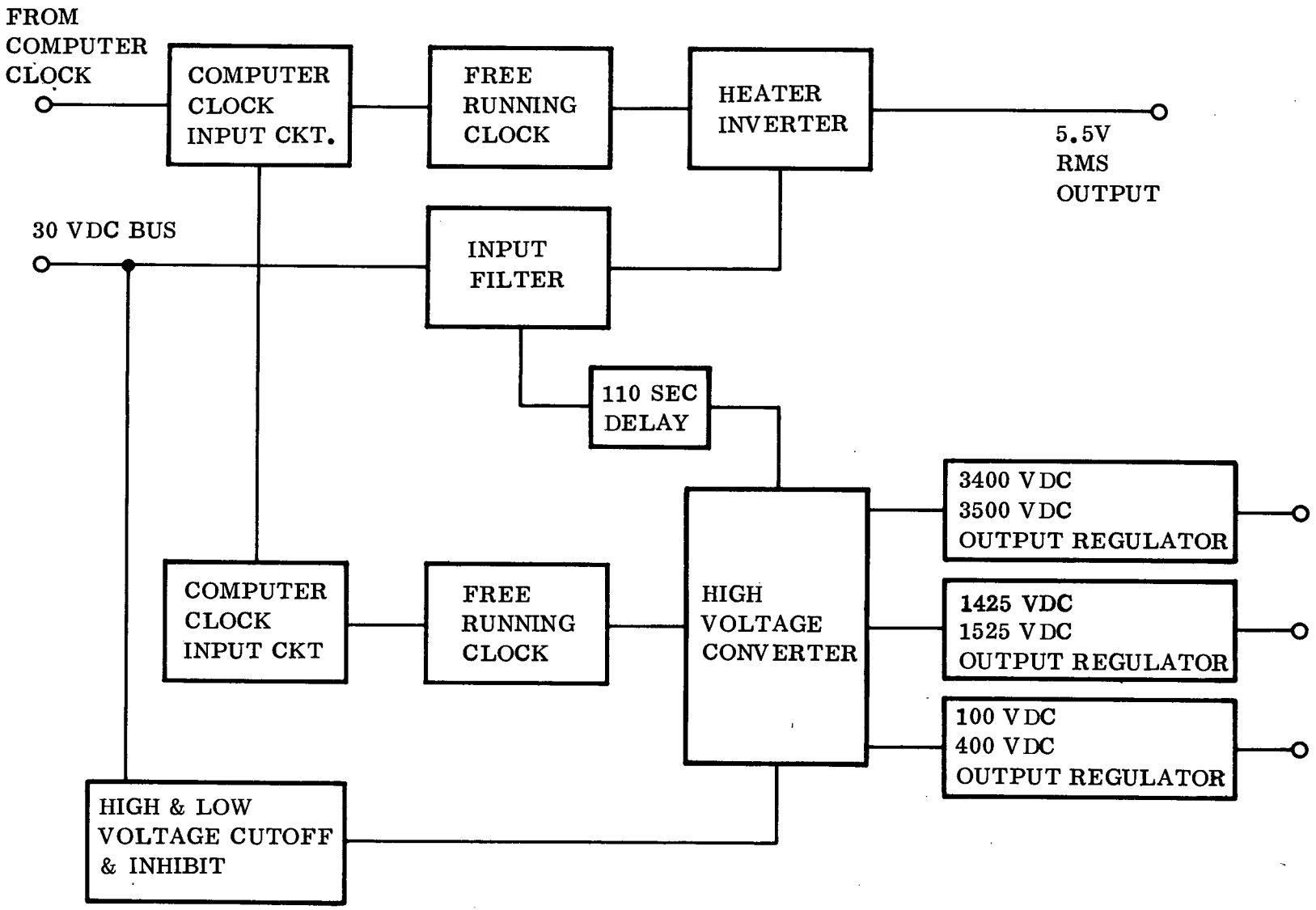


Figure 6.1-2. TWT DC to DC Converter Block Diagram

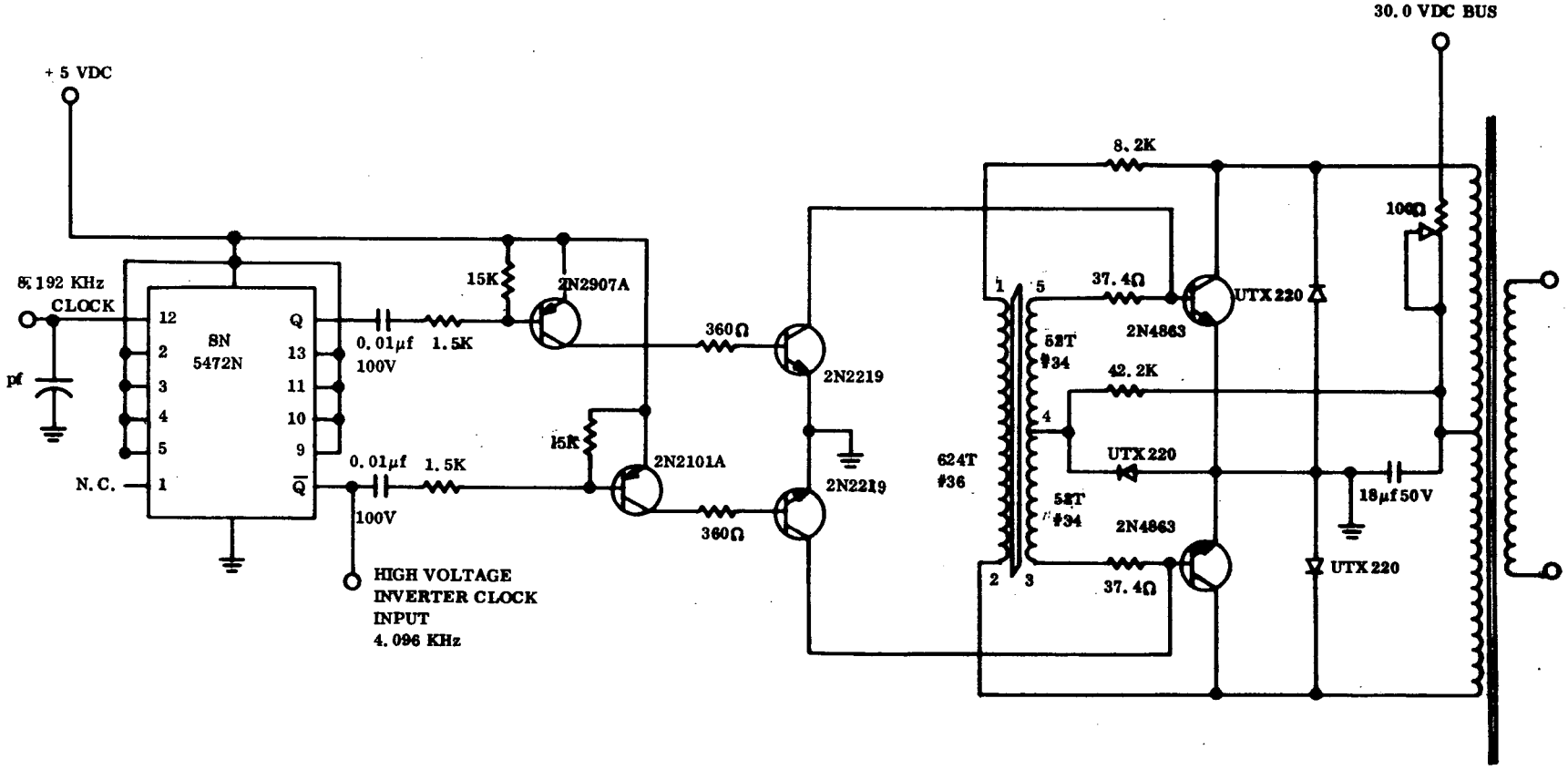


Figure 6.1-3. Heater Inverter

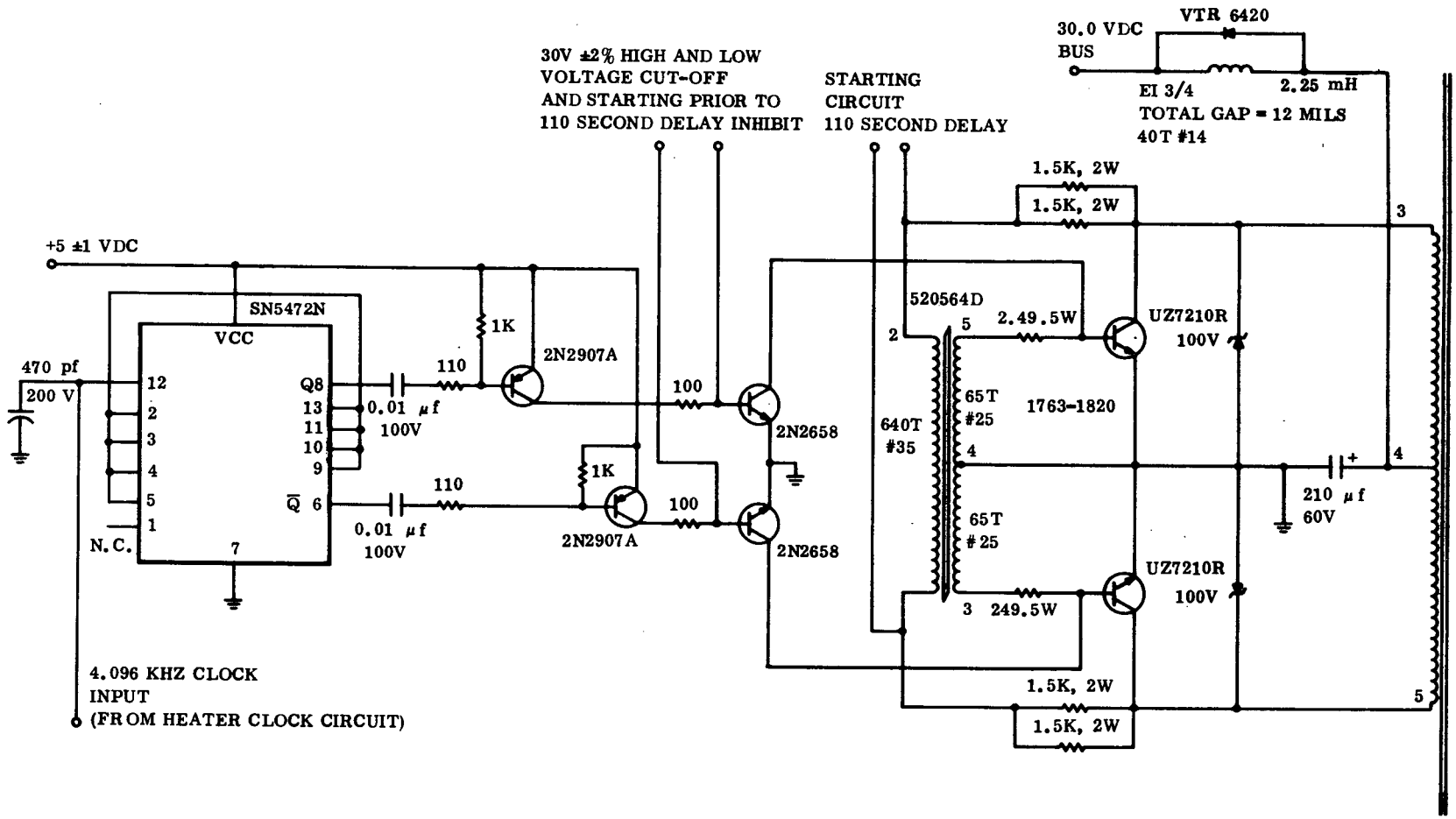


Figure 6.1-4. High Voltage Heater

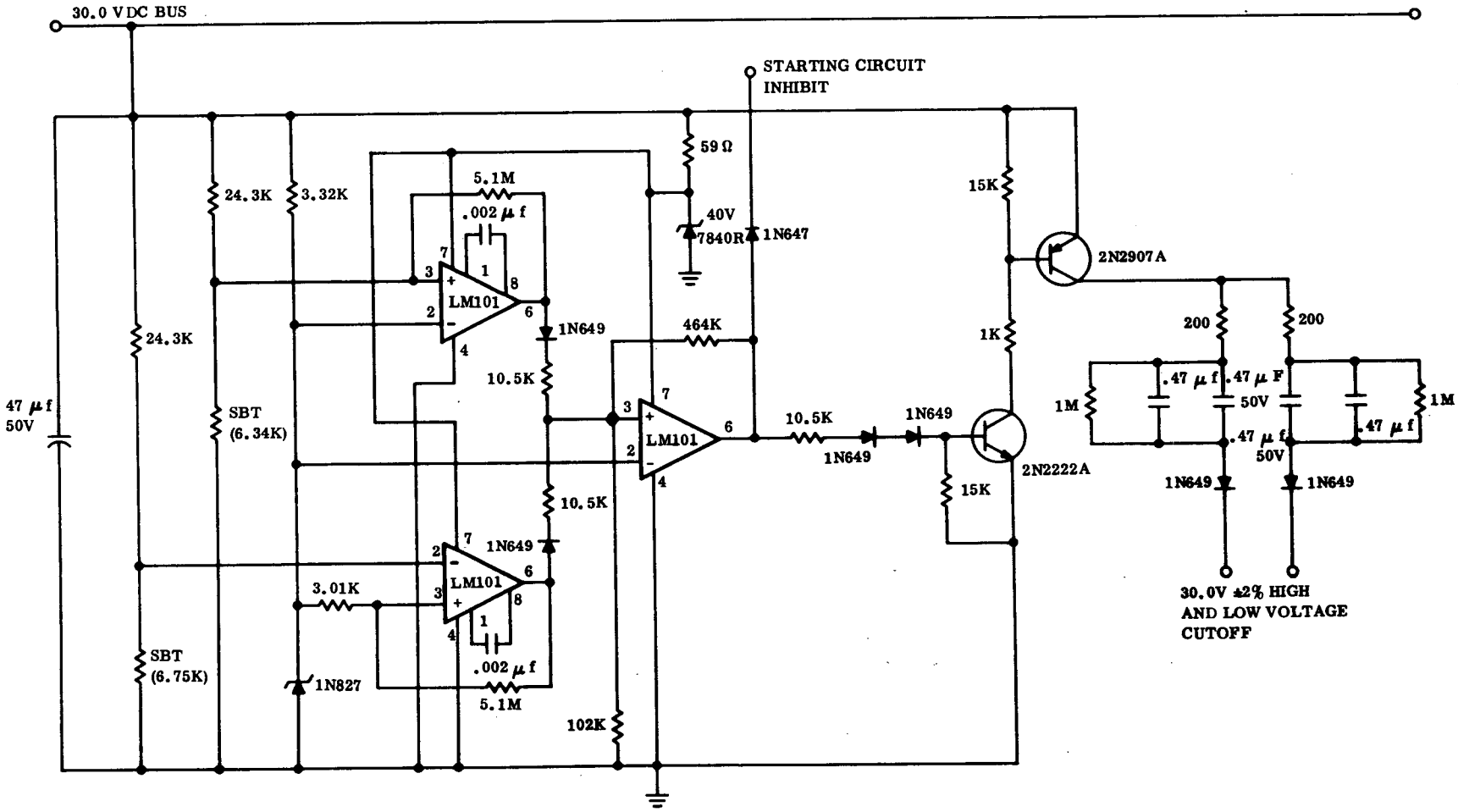


Figure 6.1-5. High and Low Voltage Cut Off and Inhibit Circuitry

voltage converter turns off if the input bus voltage is outside the 30.0 ± 2 percent voltage band, and it has to be restarted again. It also prevents the converter from turning on (inhibits) if the bus voltage is outside the described voltage band.

The circuit in Figure 6.1-6 provides a 110 second starting delay to the high voltage converter. During this period of time, it also inhibits the converter from starting due to some transient condition. The starting circuit excites the primary of the saturable core free running clock for several cycles (for a period of 50 milliseconds) thus starting the switching of the power transistors.

The high voltage transformer provides the helix, collector and anode outputs. The description of this transformer is in the High Voltage Power Transformer Section. Each one of the three outputs is rectified and filtered to provide the specified output ripple. The outputs are further regulated by their respective high voltage series regulators. The three regulators are shown in Figures 6.1-7 through 6.1-9. The regulators float on a high voltage resistive divider network (providing a constant current) and only sample portion of the output error signal. The output voltage of the helix and collector regulators is 60 volts and the anode regulator is 40 volts.

To adjust the output voltages for the specified range, the following change in the resistor dividers will provide the approximate desired output:

Helix	Collector	Anode
2.25 K ohms/volt	950 ohms/volt	2.15 K ohms/volts

To turn the TWT Power Supply on, 30 volts dc has to be applied to the input and it is recommended that the high voltage outputs be loaded to their respective loads.

A full schematic of the power supply is shown on Figure 6.1-10.

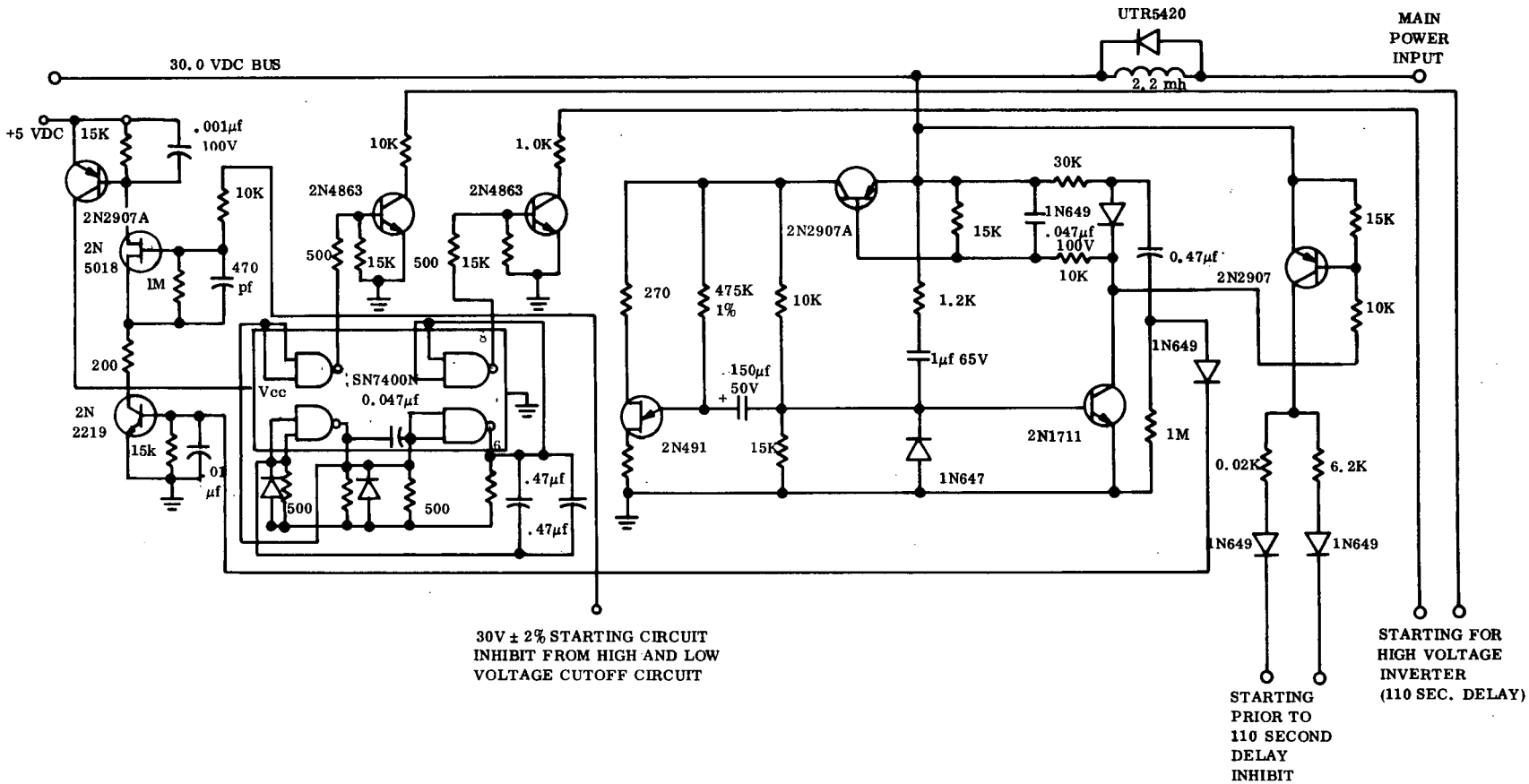


Figure 6.1-6. High Voltage Inverter Starting Circuit

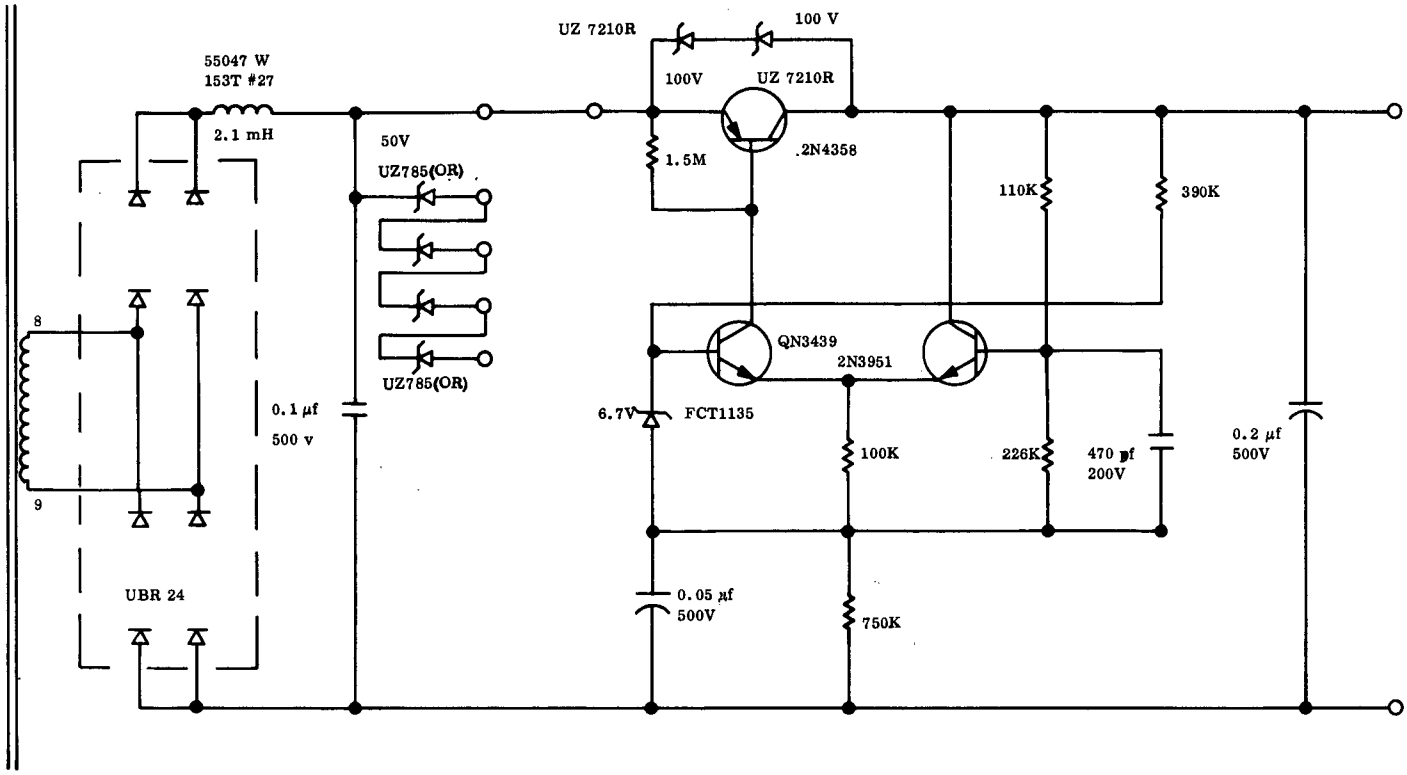


Figure 6.1-7. Anode Circuitry

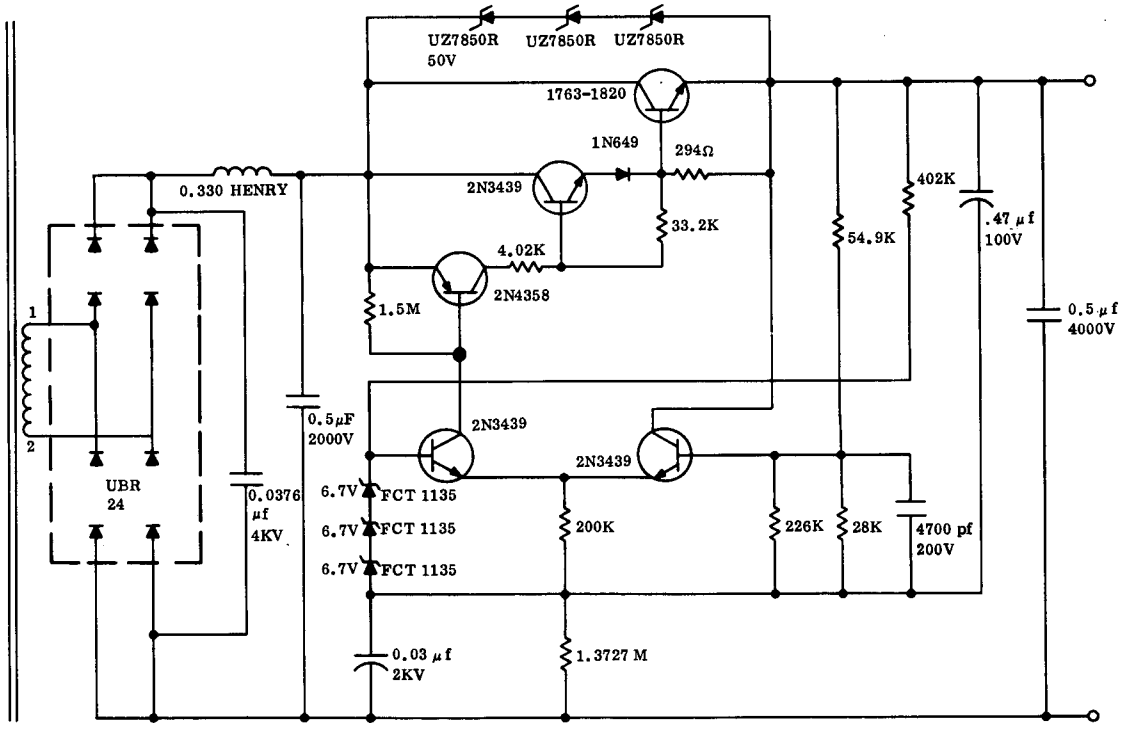


Figure 6.1-8. Collector Circuitry

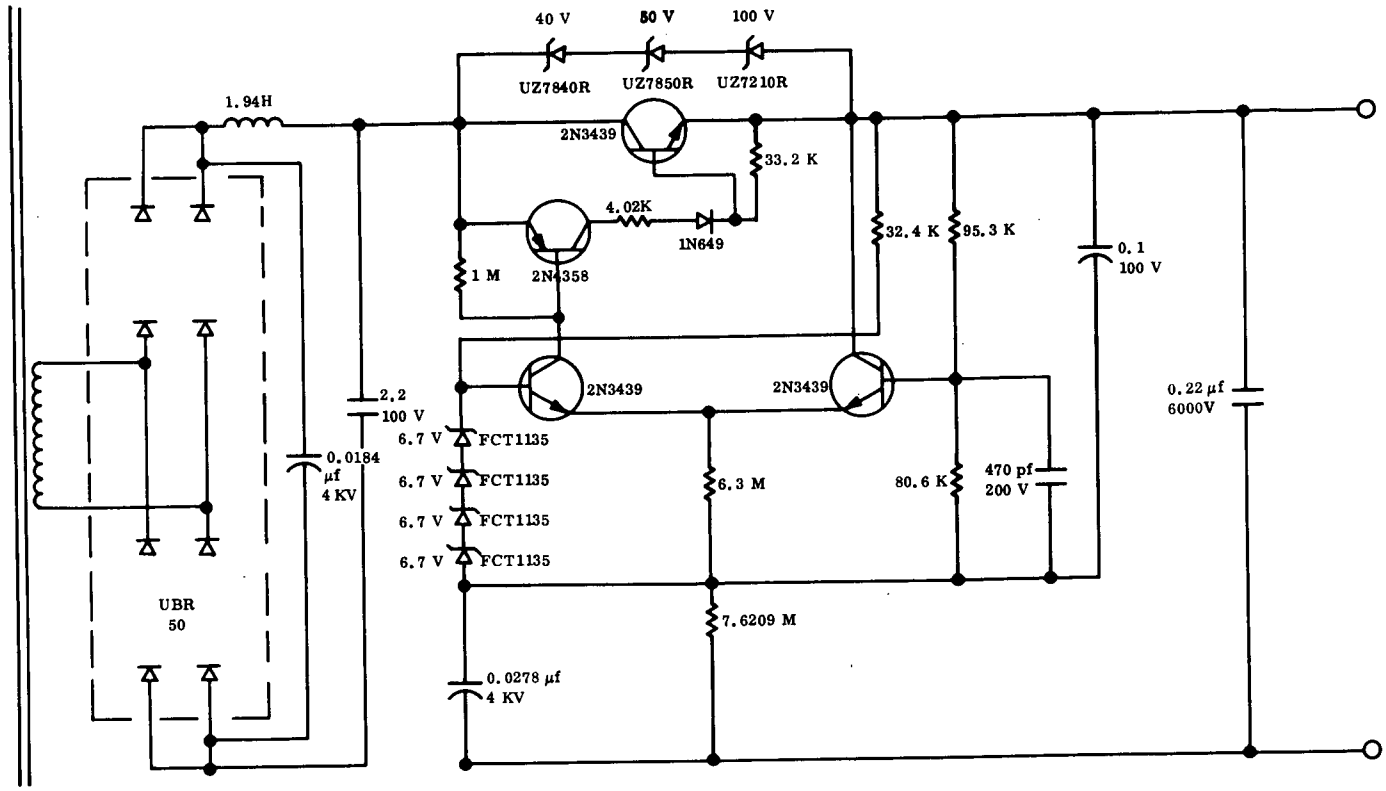


Figure 6.1-9. Helix Circuitry

The operating characteristics are listed in Table 6.1-2. They provide a quick description of the TWT Power Supply for evaluation against the specified requirements on Table 6.1-1.

6.1.2.2 High Voltage Power Transformer Design

The high voltage power transformer was designed to sustain an input voltage of 30 volts and deliver three outputs (@ 3500 volts, 1525 volts and 400 volts) with a maximum stepup ratio of 1:120. The power handling capacity of this transformer is about 100 watts, the switching frequency is 2 Kilohertz, and a flux density of 6.25 Kilogauss. The transformer efficiency is about 92.5 at full rated power. The transformer losses are divided into 5.5 watts core loss and 2 watts copper loss (@ approximately 5.5 core loss and 2 percent copper loss). The total transformer weight is 2.25 pounds.

A one mil tape Supermalloy cut "C" core was especially ordered from The Arnold Engineering Company. This material has about 1/6 the core loss of a 1 mil Selectron cut "C" core. Other transformer designs have been considered and also built, but this particular winding sequence and core material seemed to provide the maximum efficiency and minimum noise.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

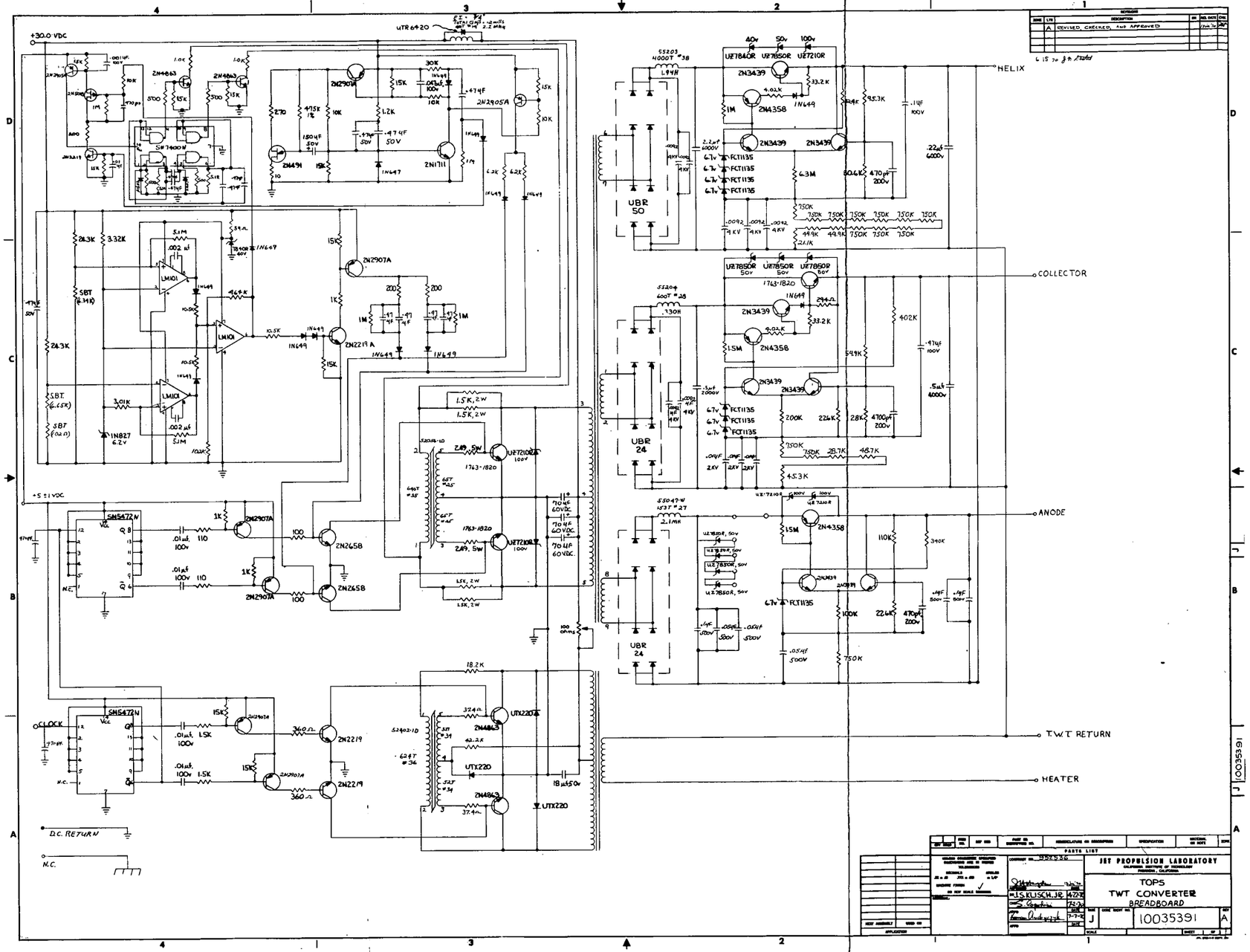


Figure 6.1-10. TWT Converter Breadboard Schematic

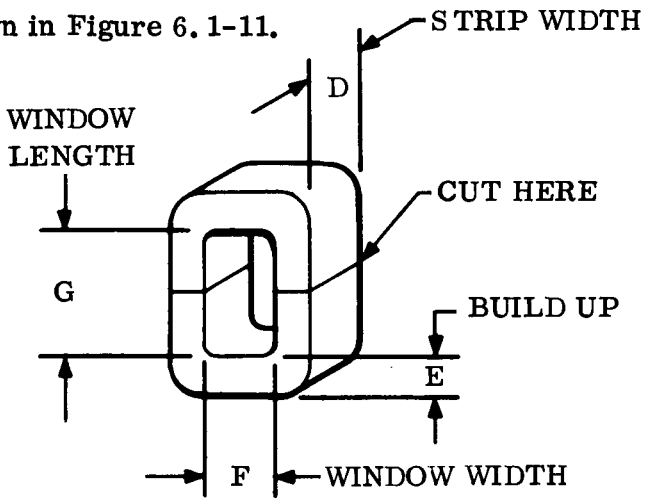
Table 6.1-2. Operating Characteristics of the TWT DC-to-DC Converter

Output	Voltage	Current	Voltage Deviation	Regulation	Ripple	Free Running Frequency
Heater	5.5 vrms	0.22 amps	+150 mv -150 mv	$<\pm$ 3%	Square Wave	3.958 kHz to 3.768 kHz
Helix	3460 vdc	2.0 to 5.0 ma	+12.7 v -19.6 v	$<\pm$ 0.5%	0.7 Vpp	1.973 kHz to 1.874 kHz
Collector	1511.2 vdc	43.0 to 48.0 ma	+1.5 v -1.8 v	$<\pm$ 0.15%	1.8 Vpp	1.973 kHz to 1.874 kHz
Anode	391.84 vdc	0.2 ma	+1.6 v -1.3 v	$<\pm$ 0.5%	0.7 Vpp	1.973 kHz to 1.874 kHz

Heater Current Limit = 0.44 amperes rms
Over Voltage Cutoff 30.704 to 30.732 vdc
Under Voltage Cutoff 29.304 to 29.254 vdc

- Temperature Change of -20°C to +80°C
- Vehicle Clock to Free Run
- Input Voltage Change of 30.0 v $\pm$ 1%
- Typical Efficiency 87%
- Total Breadboard Weight 7 lbs → Packaged 9 lbs
- Volume 240 - 250 $in.^3$
- Total Power Capability 100 watts
- Ripple Current Feedback = 20 Milliamperes pp
- Turn On Inrush Current 10 Amperes → di/dt 12,000 Amperes/Second
- Not Susceptible to 0.1 Vpp Power Source Ripple From 5 Hz to 150 kHz
- Numberical Reliability
  Lambda Per Million Hours = 10.182
- Methods of Improving the Efficiency
  - Reduce power transformer core size
  - Provide secondary transformer taps (Thus reduce voltage drop on high voltage series pass element regulator transistors).
  - Eliminate high voltage regulator divider resistors and use the output transformer taps to float the regulators.
  - All of these methods would raise the typical efficiency to about 93%.

The core specifications are shown in Figure 6.1-11.



Weight per Core	Core Dimensions (inches)				Gross Area (DXE) in.^{2}	Window Area (FXG) in.^{2}
	D	E	F	G		
0.83 lbs	3/4	1/2	$1\frac{7}{16}$	$2\frac{9}{16}$	3/8	3.7

Figure 6.1-11. Core Specifications

Two cut "C" cores were used in order to minimize the step up ratio (@ reduce it to 1:60). The primary 30 turns of AWG 23BIFILAR were connected in parallel on both sides of the single core legs and further in parallel between the two cores. The secondary windings were connected in series between both sides of the single core legs and further in series between the two cores.

The two legs of the "C" core were wound in order to cover both air gaps (this is a natural air gap of 2 mils), thus increasing the efficiency of the transformer by absorbing the energy across the air gap, due to fringing into the copper wire.

The method of sandwiching the secondary windings between the primary winding decreases the leakage reactance and increases the coupling between the primary and secondary windings. Another method used to increase coupling was to keep the width of the turns on the primary and secondary the same, this at the same time maintains the same winding margin.

In order to prevent corona, a 20 volt per mil of mylar insulation was used. Also a winding margin of 3/8 inch was used to prevent high voltage breakdown between the magnet wire and the core. The winding and interconnection method is shown in Table 6.1-3.

Table 6.1-3. Winding and Interconnection Method

Winding	Total No. Turns	Total DC Resistance
N_1 thru N_8	30 to CT	0.13 ohms to CT
N_9 thru N_{12}	3600	1757 ohms
N_{13} thru N_{16}	1600	110 ohms
N_{17} thru N_{20}	424	36 ohms

Interwinding capacitance and interlayer capacitance were kept at a minimum by selecting a flux density as high as feasible (and yet maintaining a high efficiency) in order to increase the volts per turn. A core was selected with a winding length as long as necessary in order to minimize the amount of layers required.

All good design practices known were used to increase coupling, reduce leakage reactance, reduce interwinding and interlayer capacitance, optimize size, weight and efficiency, with a certain degree of compromise used in all these conflicting requirements.

A schematic of the transformer is shown in Figure 6.1-12.

6.1.2.3 Heater Transformer

A high reactance transformer was used to provide current limiting. The sketch of the transformer is shown in Figure 6.1-3.

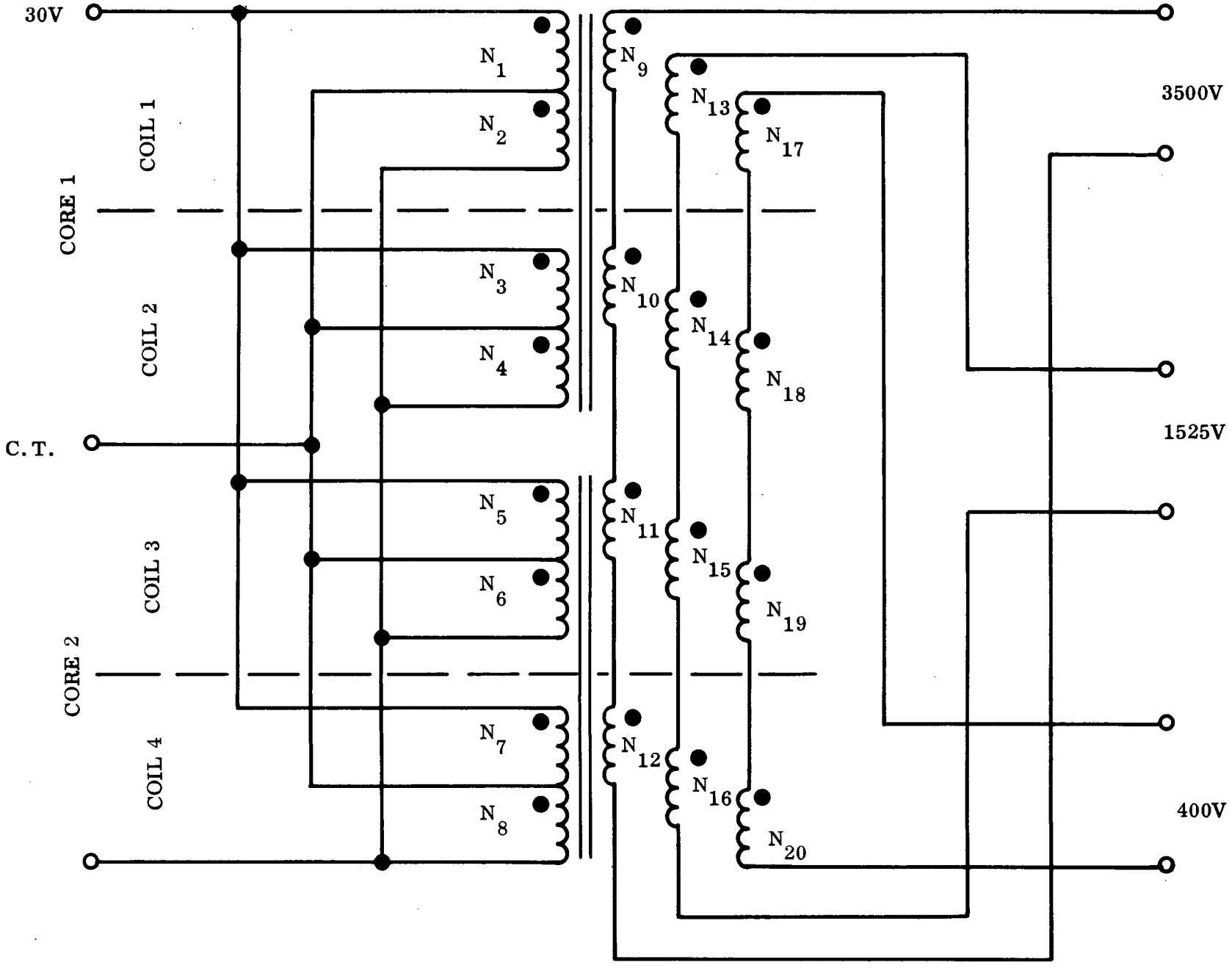


Figure 6.1-12. High Voltage Transformer

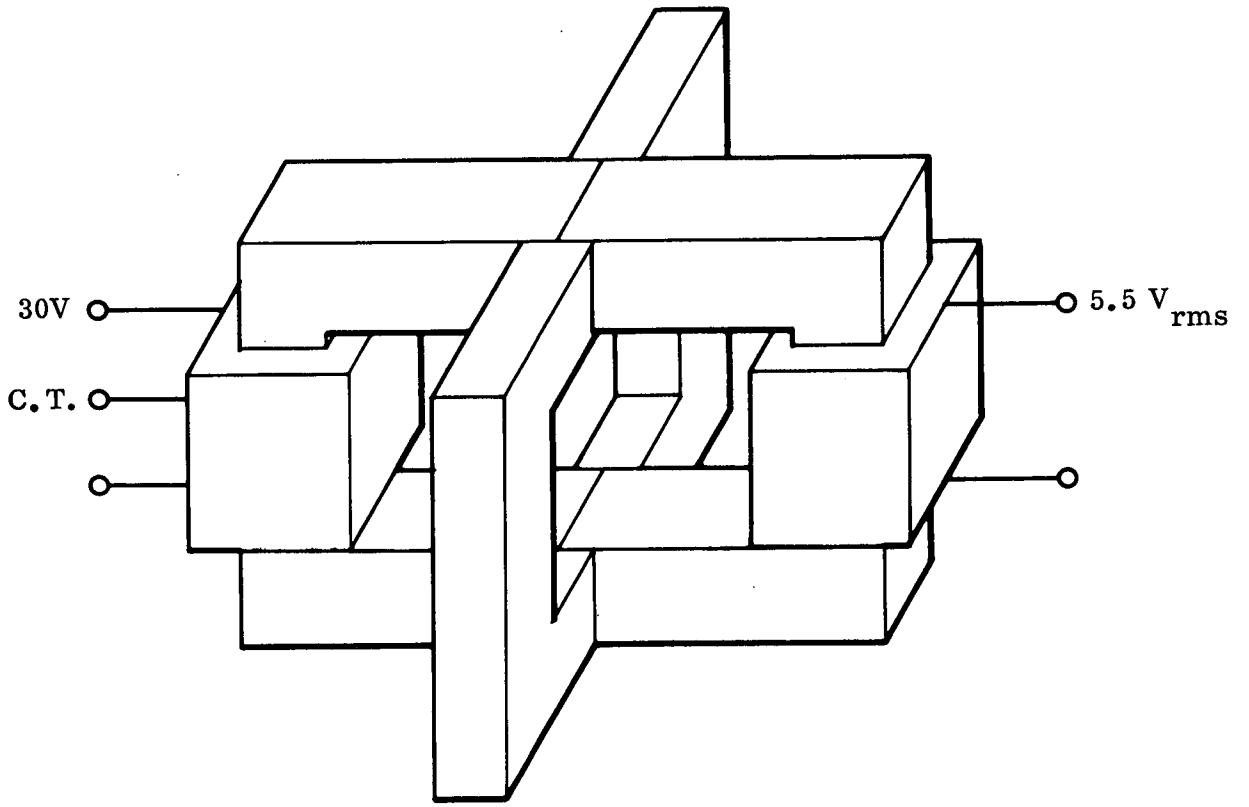


Figure 6.1-13. Heater Transformer

An AM 7 Silectron Cut "C" Core was used with the primary of 95 turns of AWG 33 on one leg of the core and a secondary of 29 turns of AWG 27 on the other leg of the core. Another "C" core AM 21 was used to introduce another flux path. All the air gaps used were the natural 1 mil air gap created by the cores.

As the secondary current increases the flux path changes direction (following the lowest resistance path) from the core with the windings to the shunting core, thus limiting the current at the output.

A test of this design showed an operating point of 5.0 to 5.5 volts rms adjustable and a short circuit current of 420 to 440 milliamperes rms.

6.2 TWO-PHASE INVERTER ASSEMBLIES

6.2.1 FUNCTIONAL CHARACTERISTICS

- Provides conversion from dc to two phase ac for gyros and momentum wheels.
- Requirements:

	Gyros	Wheels
Power rating, continuous	12 watts	12 watts
Power rating, peak	20 watts	12 watts
Frequency	1600 Hz	400 Hz
Electrical configuration	3 wire	4 wire
Command logic	5 v TTL	5 v TTL
Phase reversal	No	Yes
Inhibit override	None	200 ms pulses
Free run	Yes	Yes
Output isolation	Yes	Not required
Output voltage	25 vac ±5%	26 vac ±5%
Free run frequency	1590 Hz +0, -4%	396 Hz +0, -4%
Frequency stability	±0.5%	Not required

6.2.2 DESIGN DEFINITION

Separate two-phase inverters for the gyros and momentum wheels were design as described below:

6.2.2.1 Gyro Inverter

The Gyro Inverter is designed to provide two phase, three wire, square wave voltage at 25 volts ac rms plus or minus five percent, with a ninety degree phase displacement. A block diagram of the basic inverter is shown on Figure 6.2-1; the electrical schematic is shown on

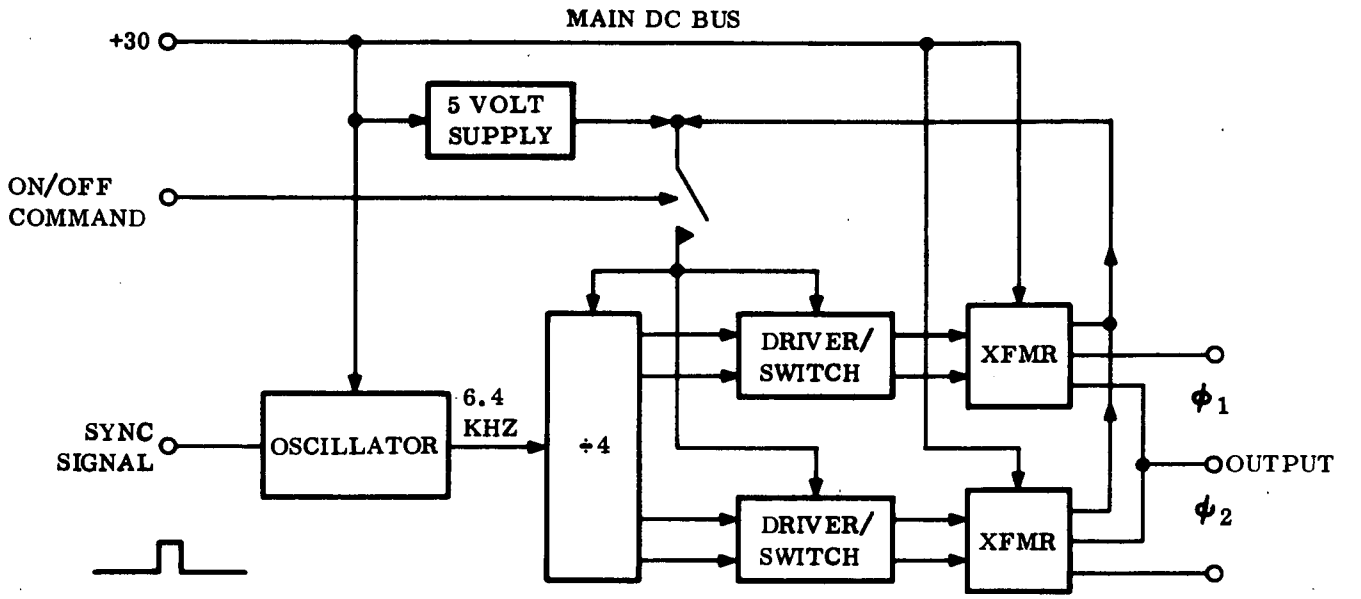


Figure 6.2-1. Gyro Inverter Block Diagram

Figure 6.2-2. Timing at 1600 Hertz is provided by an internal oscillator driven from the vehicle clock, with a back-up capability to free run at 1590 Hertz, plus zero, minus four percent if the vehicle clock is disabled. The inverter delivers six watts per phase at greater than 85 percent efficiency into a lagging power factor load of 0.9 to 1.0. Specified voltages are maintained for loads with lagging power factors of 0.5 to 1.0. On-off control by command and clock logic uses five volt TTL (Transistor-Transistor Logic) signals. The inverter operational temperature limits are from $0^{o}C$ to $40^{o}C$; non-operational limits are from $-20^{o}C$ to $+80^{o}C$.

6.2.2.2 Wheel Inverter

The Wheel Inverter is designed to provide two phase, four wire, square wave voltage at 26 volts ac rms plus or minus five percent, with a ninety degree phase displacement. A block diagram of the basic inverter is shown on Figure 6.2-3; the electrical schematic is shown on

FOLDOUT FRAME 1

FOLDOUT FRAME 2

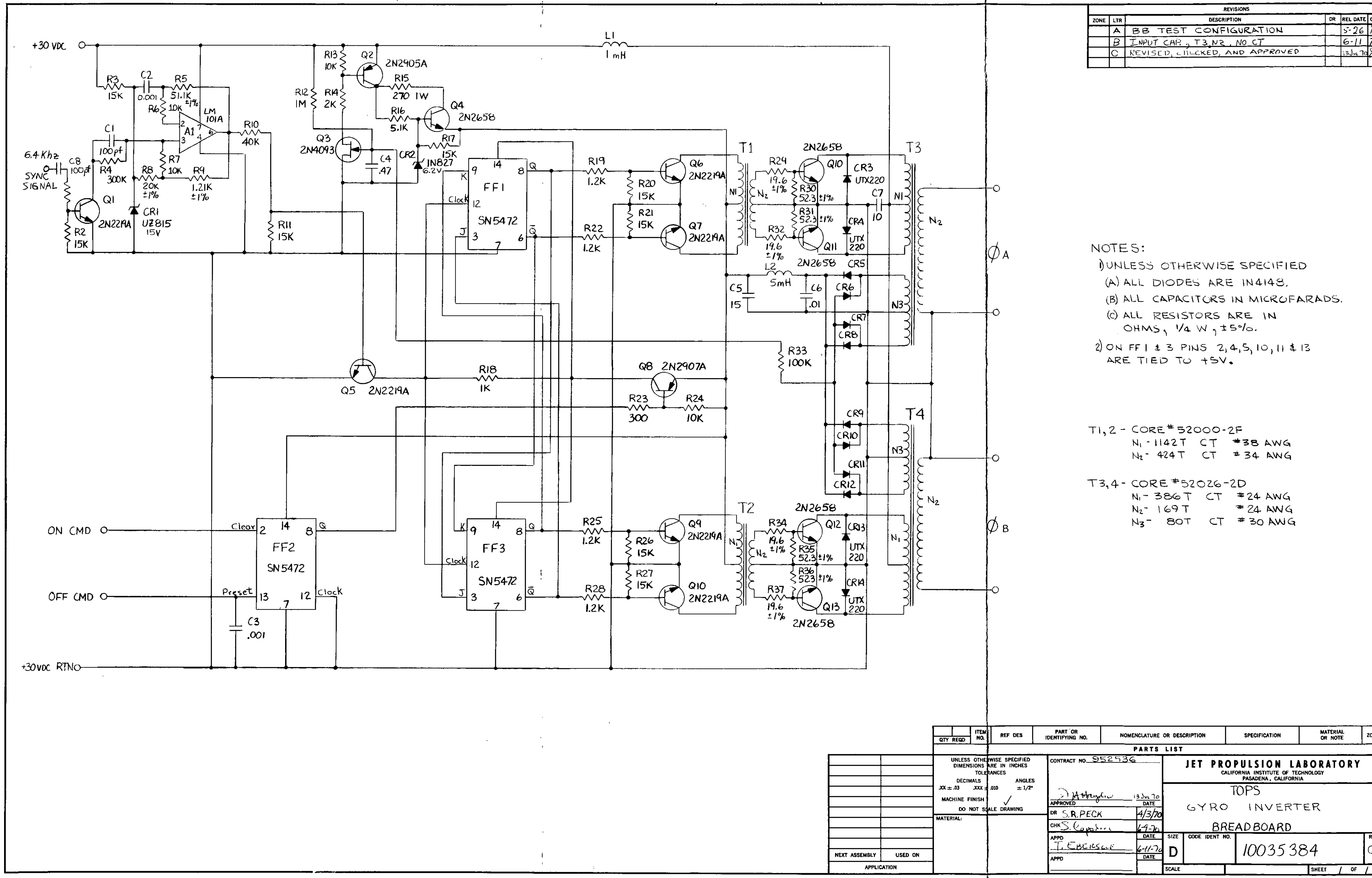


Figure 6.2-2. Gyro Inverter Breadboard Schematic

6-23

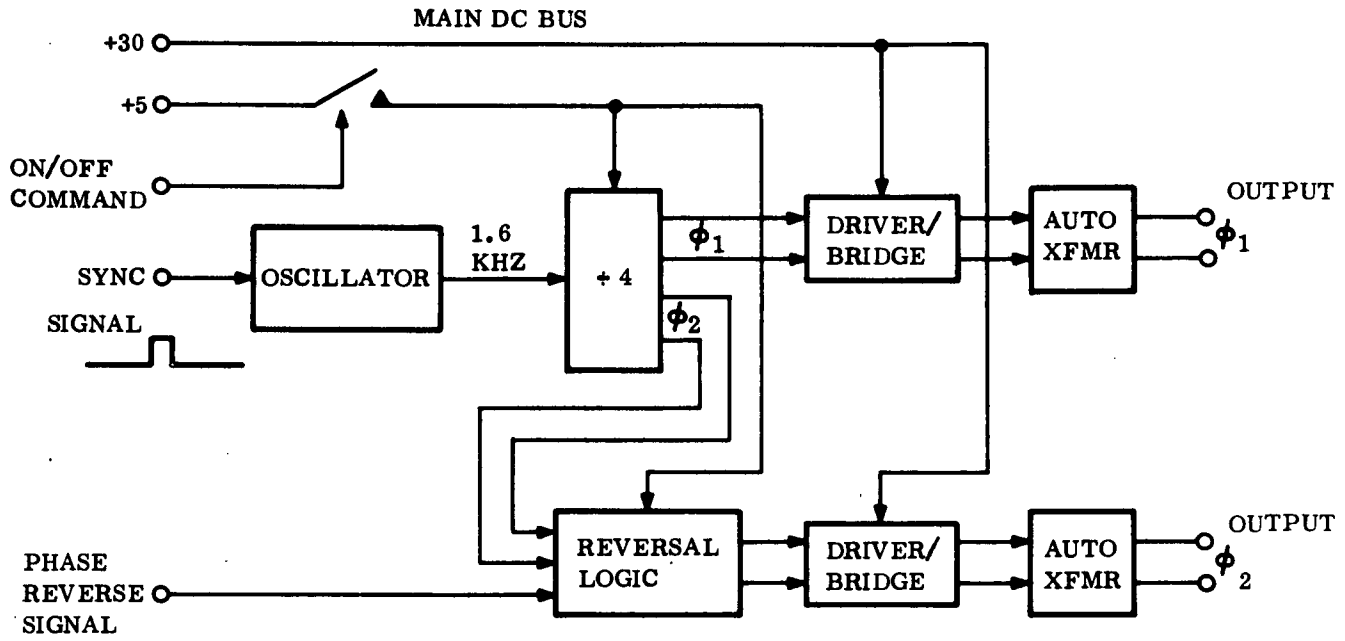


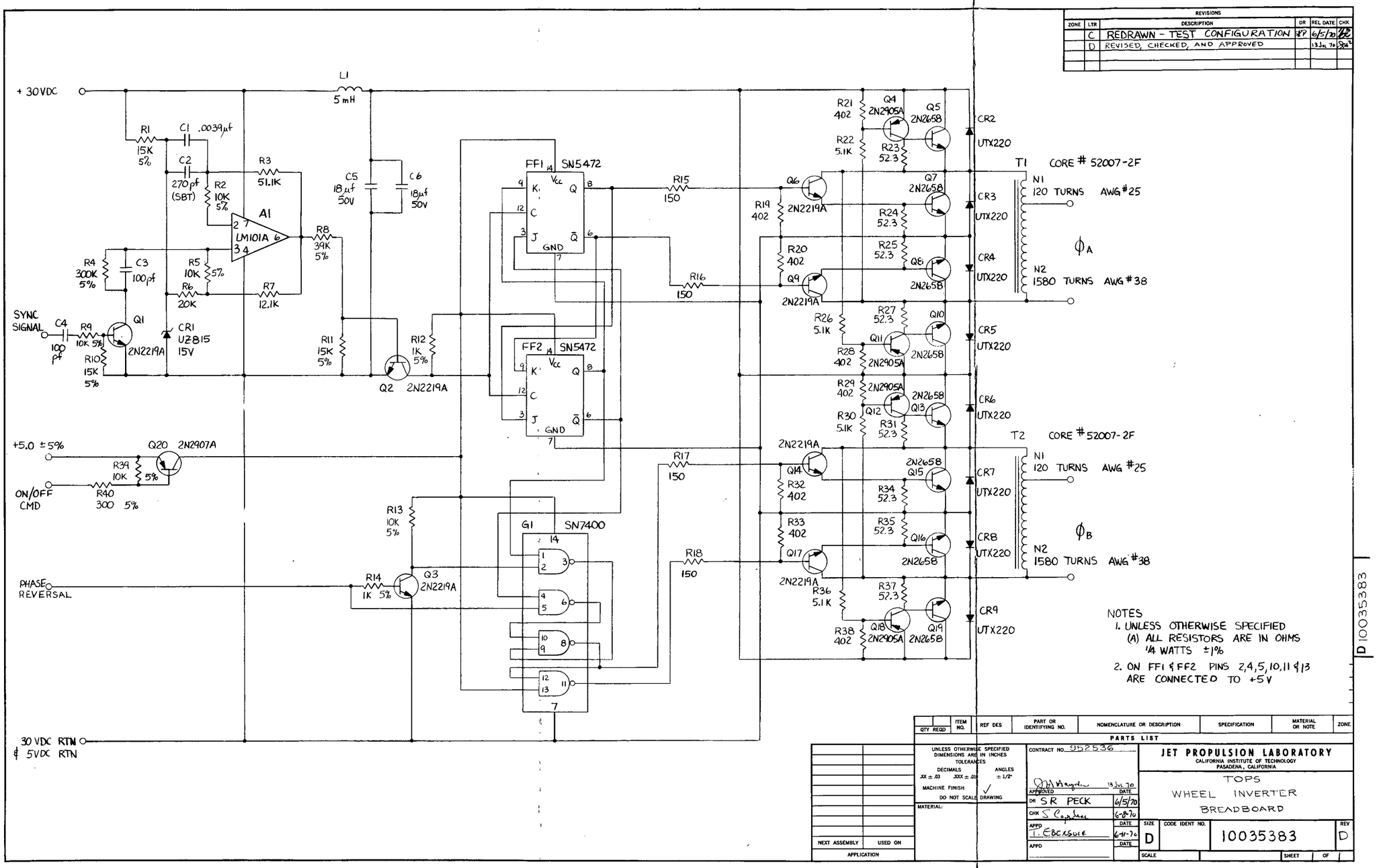
Figure 6.2-3. Wheel Inverter Block Diagram

Figure 6.2-4. Timing at 400 Hertz is provided by an internal oscillator driven from the vehicle clock, with a back-up capability to free run at 396 Hertz, plus zero, minus four percent if the vehicle clock is disabled. The inverter operates from 30.0 vdc plus or minus one percent and a 5.0 vdc plus or minus five percent logic supply. The inverter delivers six watts per phase at greater than 85 percent efficiency into a lagging power factor load of 0.9 to 1.0, and provides the specified voltage into lagging power factor loads of 0.5 to 1.0. Command signals control the on-off or phase reversal state of the inverter. All command and clock logic uses five volt TTL (Transistor-Transistor Logic) signals. Normal ON command uses a 200 millisecond pulse with a repetition rate from zero to five per second. The inverter is required to operate in specification from $0^{o}C$ to $40^{o}C$; non-operational limits are from $-20^{o}C$ to $+80^{o}C$.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS					
ZONE	LTR	DESCRIPTION	DR	REL DATE	CHK
	C	REDRAWN - TEST CONFIGURATION	SP	6/5/70	BE
	D	REVISED, CHECKED, AND APPROVED		13 JUL 70	SRP



NOTES
1. UNLESS OTHERWISE SPECIFIED
   (A) ALL RESISTORS ARE IN OHMS
   ¼ WATTS ±1%
2. ON FF1 & FF2 PINS 2,4,5,10,11 & 13 ARE CONNECTED TO +5V

QTY REQD	ITEM NO.	REF DES	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	MATERIAL OR NOTE	ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS: XX ± .03, XXX ± .010
ANGLES: ± 1/2°
MACHINE FINISH ✓
DO NOT SCALE DRAWING
MATERIAL:

NEXT ASSEMBLY | USED ON
APPLICATION

CONTRACT NO. 952536

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

TOPS
WHEEL INVERTER
BREADBOARD

		DATE
APPROVED	[signature]	13 JUL 70
DR S R PECK		6/5/70
CHK S Copeland		6-8-70
APPD T. EBERSOLE		6-11-70
APPD		DATE

SIZE D | CODE IDENT NO. | 10035383 | REV D
SCALE | SHEET | OF

D 10035383

Figure 6.2-4. Wheel Inverter Breadboard Schematic

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6.27

6.27.1

6.2.3 DRIVE CIRCUIT ALTERNATIVES

In developing the 2-phase inverter designs, several drive circuit alternatives were considered. A voltage of 26 volts rms was assumed with a continuous power requirement of 12 watts and a peak (stall) requirement of 20 watts at a power factor of 0.5. Input driving signals are derived from an on-board clock. Input impedance must be greater than 10 kilohms to avoid excessive loading on the input signal.

6.2.3.1 Alternative No. 1 - Direct Drive, Isolated Output (Figure 6.2-5)

In this approach, a power transformer with center tapped primary is required in each phase. The power transistors alternately switch power from one half of the primary winding to the other half. This results in having only one switch voltage drop in series with the load at any time. The darlington driver provides the most efficient means of driving the power switch directly from the clock.

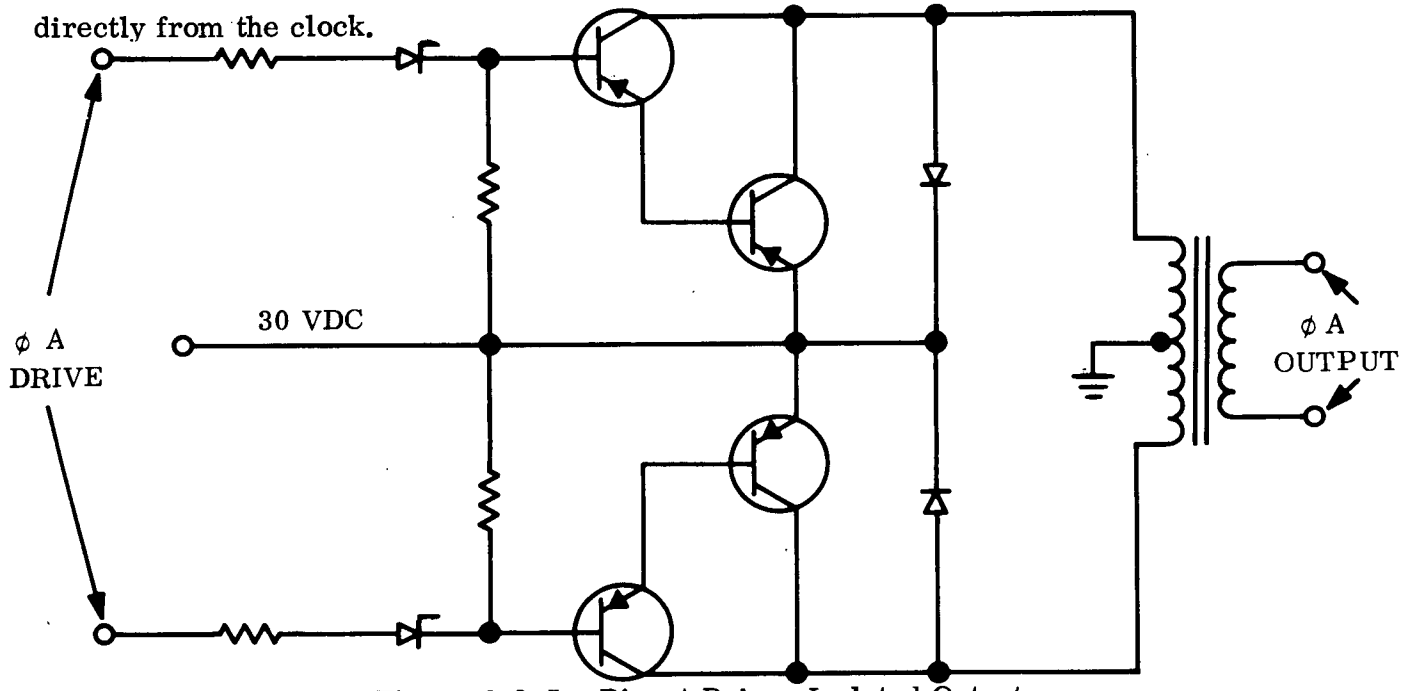


Figure 6.2-5. Direct Drive, Isolated Output

6.2.3.2 Alternative No. 2 - Isolated Drive, Direct Output (Figure 6.2-6)

The initial stage in this circuit operates exactly as does the circuit of Figure 6.2-5. However, the transformer supplies base drive to a transistor bridge circuit instead of the load. The resulting reduction in required source current eliminates the need for darlington input switches.

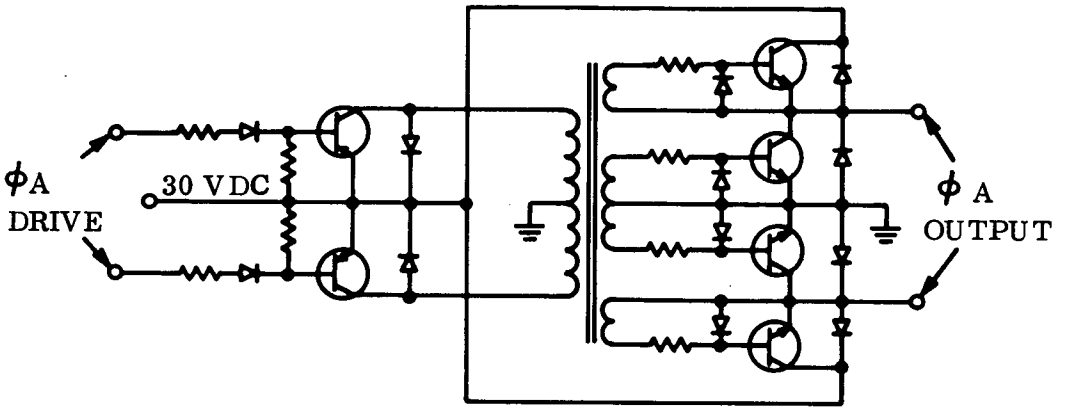


Figure 6.2-6. Isolated Drive, Direct Output

The bridge provides the required ac by alternately switching power and returns through two transistors at each end of the load. Thus, there are two saturation voltage drops in series with the load at any time. However, the rms voltage delivered to the motor is equal to the source minus two transistor voltage drops, or approximately 29.0 vac rms. A second consideration is that both ends of the motor winding must be isolated, since each is alternately connected directly to the 30 volt bus.

6.2.3.3 Alternative No. 3 - Direct Drive, Direct Output (Figure 6.2-7)

In this circuit, the signal input is applied directly to an NPN darlington pair which forms the bottom leg of the bridge. The top leg, consisting of a PNP darlington pair, receives its drive from the corresponding bottom switch. In this manner, the need for a transformer is eliminated. However, each switch requires a darlington configuration which results in a higher saturation voltage drop than that of a single transistor (a typical drop for two transistors would be 1.5 to 2 volts). Also, as in the output bridge of circuit 2, there will be two switch voltage drops in series with the load at all times. This circuit more nearly matches the 26 vac rms motor requirement, but still requires isolated motor windings.

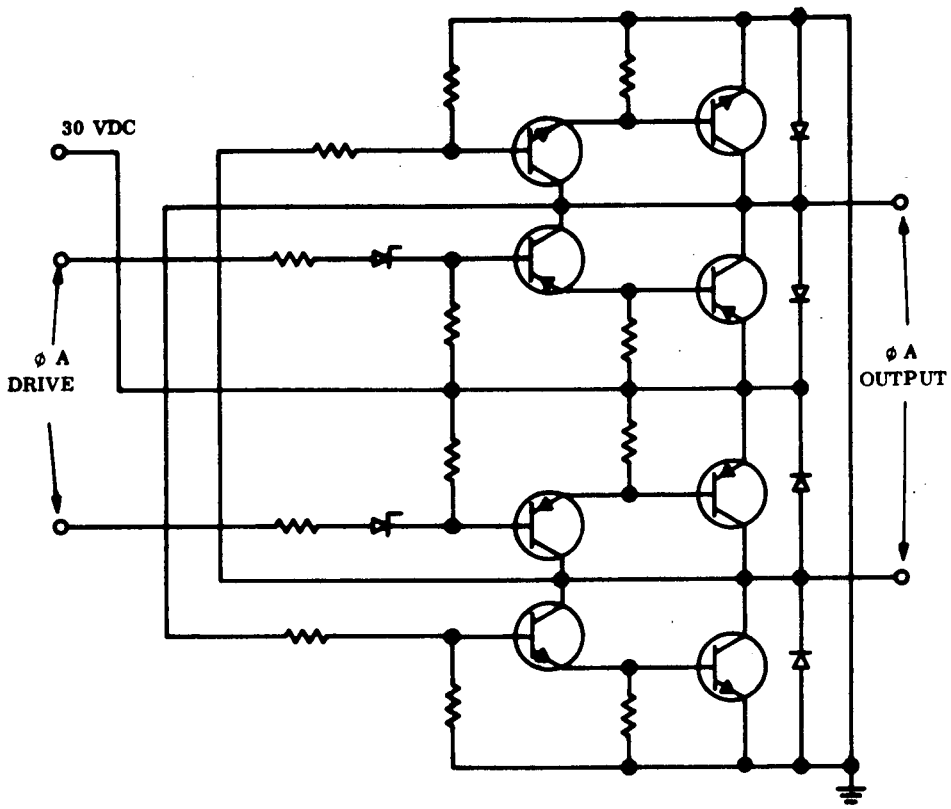


Figure 6.2-7. Direct Drive, Direct Output

6.2.3.4 Tradeoff Characteristics

The circuit of Figure 6.2-5 offers the following major advantages:

(1) Low complexity

(2) Output voltage flexibility

(3) Isolation

(4) High efficiency

The low complexity indicates a high reliability; however, any increase in reliability is offset to some extent by the very high failure rates usually applied to magnetic components. The output flexibility and isolation advantages would seem to be of importance in this particular application since the gyro requires approximately 26 vrms and is a three wire device.

The efficiency of this circuit approaches 90 percent; however, it should be remembered that the magnitude of the losses in this application is very small -- approximately 60 mw per percent of efficiency. Therefore, any efficiency greater than perhaps 85 percent would be acceptable.

The major disadvantage of this approach is the size and weight of the power transformers. The two six watt transformers required (one each phase) could weigh up to one-half pound and would account for most of the total supply weight.

In the circuit of Figure 6.2-6, the transformer provides base drive for the transistor bridge. If a forced gain of 10 (the usual value for power switches) is used, the transformers must provide one tenth as much power. Since the primary voltage is constant, the only factor contributing to a reduction in size is less current -- therefore, smaller wire. The number of primary turns will be equal to or greater than (for a smaller core) that of the power transformer. The total number of secondary turns would be no less than half of the power transformer approach. The net result is that a driver transformer will be at least half the size of a power transformer. Since additional power transistors are required, the overall size and weight of this circuit will be approximately the same as that of Figure 6.2-5.

The attractiveness of the circuit of Figure 6.2-6 is further reduced by the increased complexity (approximately 3 times that of Figure 6.2-5) required in the bridge output. This would cause a substantial decrease in the reliability figure of merit. Another factor affecting reliability is the lack of dc isolation. Any bridge circuit is highly vulnerable to failure due to inadvertent grounding of either output terminal.

The efficiency of the circuit of Figure 6.2-6 would be slightly better than that of the first circuit even though there are two switches in series with the load. This is due to the single transistor voltage being less than one half that of a darlington. The efficiency increase, however, would be small.

The output voltage of a bridge inverter is reasonably fixed at something less than the bus voltage. In the circuit of Figure 6.2-6, it would be about 29 vrms. In the forced gain configuration, the saturation drop will not change significantly over a fairly wide load range (say 5 to 1). The output voltage regulation will, therefore, be better than 5 percent from stall to running loads.

The circuit of Figure 6.2-7 has a complexity similar to that of Figure 6.2-6; however, the reliability will be better due to the lack of a transformer. The output voltage will be about 28 vrms due to the greater saturation voltage drop of the darlington stages. This drop also reduces the overall efficiency to perhaps 80 percent.

The greatest advantage of this circuit is size and weight. At the required power level (6 watts per phase), this circuit would not weigh more than 3/4 pound for both phases (depending upon packaging).

6.2.3.5 Summary

In the table below, a summary of the trade-off consideration given each configuration is presented. The data pertains to a completely packaged two phase supply, but does not include input filtering.

Circuit	Size ($in.^3$)	Weight (lb)	Efficiency (%)	Regulation (%)	Reliability
Alternative 1	20	1.25	88	3	0.9243
Alternative 2	20	1.25	89	5	0.8505
Alternative 3	10	0.75	80	5	0.8541

The reliability was calculated on a part count basis using TOPS failure rates and a design life of twelve years. Alternative No. 1 appears as the best overall approach. A variation of this approach was used in the gyro and momentum wheel designs described earlier in paragraph 6.2.1.

6.3 DC POWER CONDITIONER ASSEMBLIES

To span a range of design characteristics for DC power conditioning assemblies, some representative converters were designed for the following TOPS load applications:

1. Science Data Subsystem
2. Tracking Receiver
3. DC Magnetometer

These are described separately in the following paragraphs.

6.3.1 SCIENCE DATA SUBSYSTEM CONVERTER

The Science Data Subsystem Converter provides three rectified outputs as specified in Table 6.3-1. The outputs are required to stay within the regulation limits over variations in line (30 vdc ± 1%) and temperature (0^{o}C to 40^{o}C); the converter is required to withstand and recover from temperature extremes of -20^{o}C and $+80^{o}$C. The converter has the capability of operating in either a free-running mode or in a clock driven mode. A block diagram is shown on Figure 6.3-1; an electrical schematic is shown on Figure 6.3-2.

Table 6.3-1. Output Requirements

Output Voltage (Volts)	Regulation (Percent)	Load Current (ma)	Load Power (watts)
+ 5.0	±10	3.15	15.75
+15.0	± 5	0.1	1.5
-15.0	± 5	0.1	1.5

When the vehicle clock pulse is not present, the circuit operates as a simple Jansen Oscillator at a frequency determined by the saturable transformer (approximately 7.8 KHz).

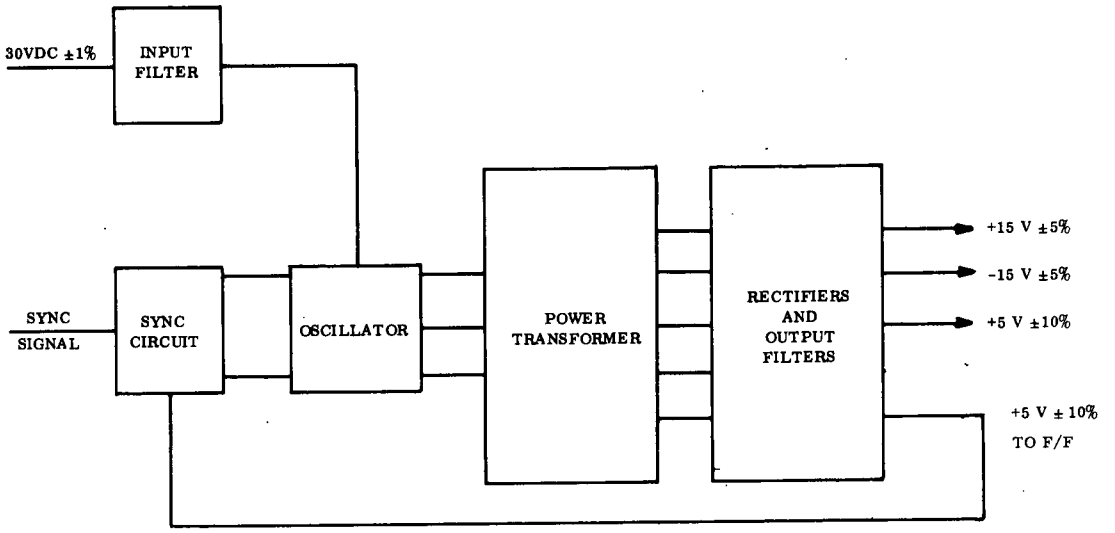
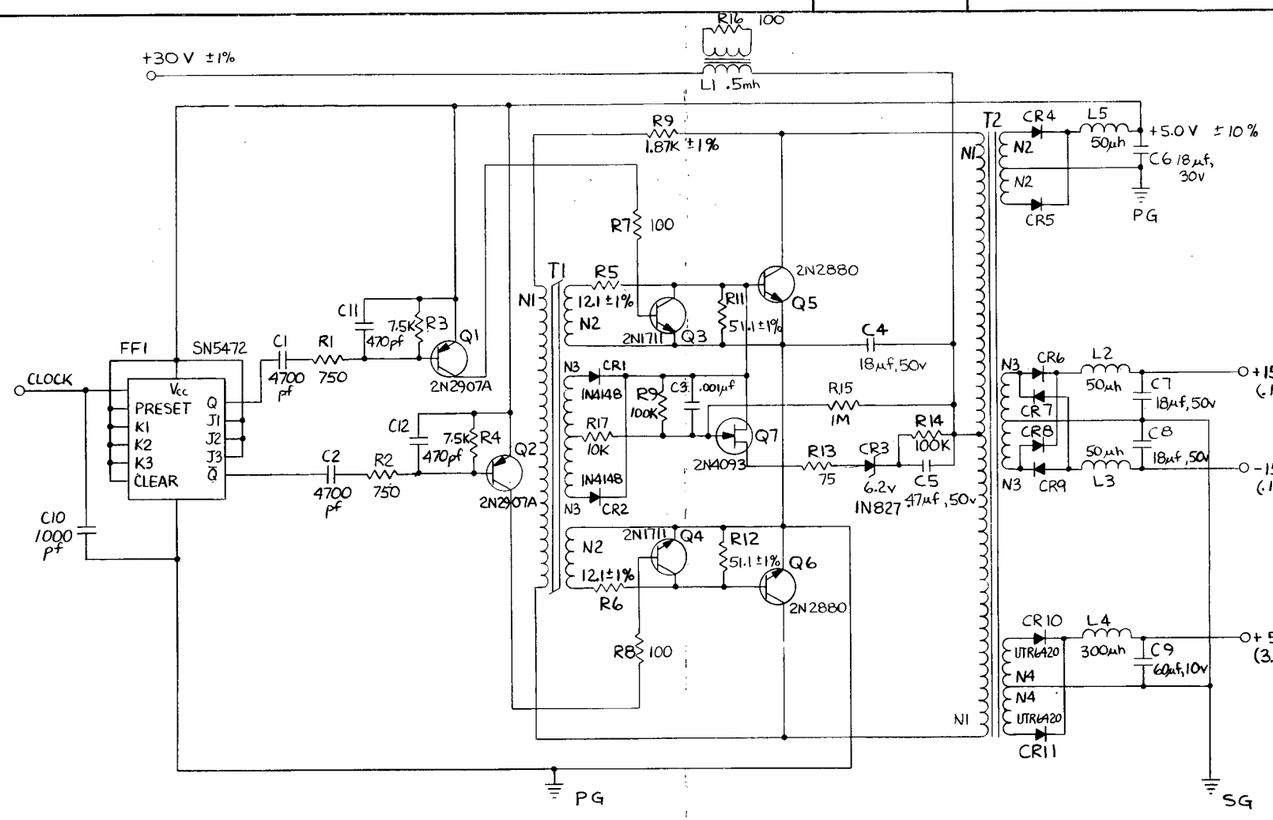


Figure 6.3-1. Science Data Subsystem Converter Block Diagram

When the vehicle clock pulse is present, the saturable transformer base drive signal is terminated prematurely in each half cycle and the switching transistors are switched at 8.2 KHz. This is accomplished with a clock frequency of 16.4 KHz where each clock pulse causes an internal flip-flop at the converter to change state. The flip-flop outputs, Q and $\overline{Q}$ are ac coupled to transistors Q1 and Q2 where Q5 is on when outputs Q and $\overline{Q}$ are "1" and "0" respectively. Prior to the switching transformer saturating and reversing polarity, a clock pulse causes the flip-flop to change state resulting in momentary saturation of Q1 and Q3, turning off Q5, and implementing the premature polarity reversal of the saturable transformer. When the transformer polarity is reversed, Q6 is turned on and the saturable transformer attempts to saturate once again. Before the transformer reaches saturation, the clock pulse changes the state of the flip-flop once again, saturating Q2 and Q4 and turning on Q5. These half cycles are repeated on each clock pulse.

FOLDOUT FRAME 1

FOLDOUT FRAME 2



REVISIONS					
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	B		SKF	6-11-70	
	C	REVISED, CHECKED, AND APPROVED		13 Jul 70	

NOTES:
1) UNLESS OTHERWISE SPECIFIED
(A) ALL DIODES ARE UTX220
(B) ALL RESISTORS ARE IN OHMS, 1/4 W, ±5%

L1 CORE # 55930
PRIMARY 57 TURNS AWG #20
SECONDARY 57 TURNS AWG #26

L2 & L3 CORE # 55051
43 TURNS AWG #22

L4 CORE # 55930
44 TURNS AWG #18

L5 CORE # 55020
32 TURNS AWG #32

T1- CORE # 50153-1D
N1 - 548 TURNS AWG #38
N2 - 21 TURNS AWG #32
N3 - 70 TURNS AWG #38

T2- CORE - AM-5
N1 - 93 TURNS AWG #22
N2 - 19 TURNS AWG #38
N3 - 51 TURNS AWG #31
N4 - 20 TURNS AWG #17

QTY REQD	ITEM NO.	REF DES	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	MATERIAL OR NOTE	ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010
ANGLES ± 1/2°
MACHINE FINISH ✓
DO NOT SCALE DRAWING
MATERIAL:

NEXT ASSEMBLY | USED ON
APPLICATION

CONTRACT NO. 952536

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

TOPS
SCIENCE DATA SUBSYSTEM
CONVERTER BREADBOARD

APPROVED		13 Jul 70	DATE
DR	S.R. PECK	4-10-70	
CHK		6-11-70	
APPD		6-11-70	DATE
APPD			DATE

SIZE D | CODE IDENT NO. | 10035386 | REV C
SCALE | SHEET | OF

D10035386

Figure 6.3-2. Science Data Subsystem Converter Breadboard Schematic

This sync-circuit acts only to turn off the on transistor (Q5 or Q6) and initiates the reversed polarity of the saturable transformer. The transformer polarity then acts to turn on the other transistor. This delay, between one transistor being turned off before the other is turned on, eliminates the possibility of current shoot-through which occurs when both transistors are on simultaneously.

The sync-circuit operates from negative going clock pulses. The pulse requirement, as presently defined, is shown on Figure 6.3-3. The fall time indicated for the negative going pulse is that which would be required to cause the flip-flop to change state.

6.3.1.1 Input Filters

A filter was designed and developed in order to control conducted emission, conducted susceptibility, transient susceptibility, and rate of current changes (di/dt) on input power lines. The configuration features a unique application of a 0.5 millihenry transformer with its primary in series with the unregulated power line. The transformer acts as an inductor and as an impedance transformer that couples a variable impedance to the primary to provide ac noise attenuation, but dissipates no dc power. The filter also includes one eighteen microfarad capacitor across the power lines. This inductor and capacitor act as a low pass filter for dc and the capacitor acts like a noise sink for ac currents generated within the converter.

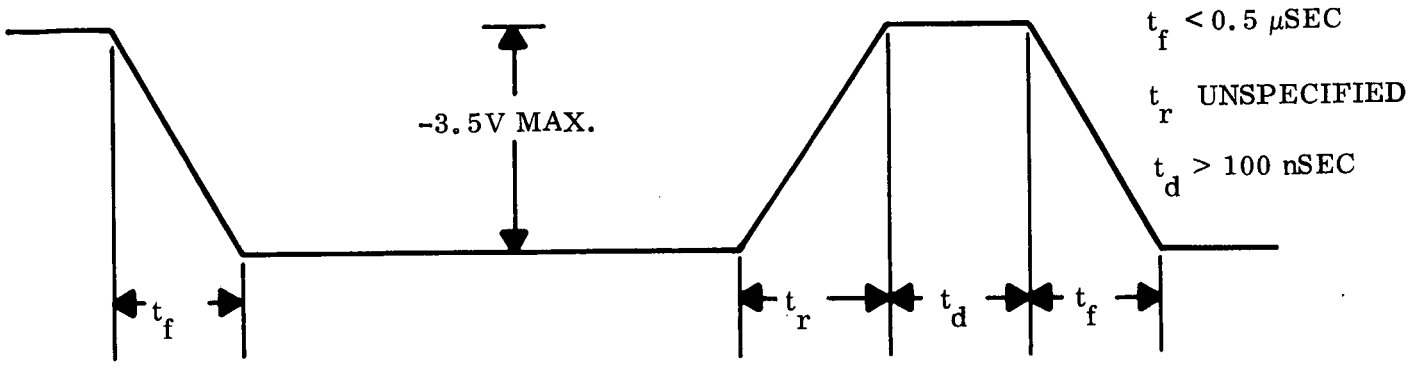


Figure 6.3-3. Clock Pulse Requirement at 16.4 Kilohertz

6.3.1.2 Inverter

The inverter is a basic Jensen oscillator with a transisitor starting circuit. T1 is a switching transformer with a square permalloy 80 core. The design of T1 and the value of the resistor R9 determine the oscillating frequency. R9 also acts to limit the current when T1 saturates. R5 and R6 limit the current to the bases of Q5 and Q6 respectively.

The transistor Q7 and the resistor R15 comprise the starting circuit which provides an initial current pulse to the base of Q5 insuring that the converter will begin to oscillate. After oscillation has begun, Q7 is back biased by a rectified output of the switching transformer, T1, and thus is turned off.

T2 is the power transformer which transforms the input voltage to the desired output levels and also provides isolation between the input and output and between outputs. A supermalloy cut core with an inherent air gap is used for T2 because this type core does not saturate and therefore does not produce large current spikes when the switching transistors are not closely matched.

6.3.1.3 Rectifying and Filtering Output

The outputs of the inverter are rectified and then passed through a passive LC filter. The filtering smooths the commutation losses during the switching intervals and restricts the ripple within the limits of the particular load requirement.

6.3.1.4 Power Supply External Sync

The power supply must be capable of accepting a sync signal from the vehicle clock to prevent beat frequencies between converters which could affect magnetometer performance.

6.3.2 Tracking Receiver Converter

The Tracking Receiver Converter provides four rectified outputs as specified in Table 6.3-2. The outputs are required to stay within the regulation limits over variations in line (30 vdc ± 1%) and temperature (0^{o}C to 40^{o}C); the converter is required to withstand and recover from temperature extremes of -20^{o}C and $+80^{o}$C. The converter has the capability of operating in

either a free-running mode or in a clock driven mode. A block diagram is shown on Figure 6.3-4; an electrical schematic is shown on Figure 6.3-5. Aside from the difference in output voltages, the design and operation of the converter is identical to that described for the Science Data Subsystem (para. 6.3.1).

Table 6.3-2. Output Requirements

Output Voltage (Volts)	Regulation (Percent)	Load Current (ma)	Load Power (watts)
+6	±2	333	2.0
-6	±2	333	2.0
+15	±2	133	2.0
-15	±2	133	2.0

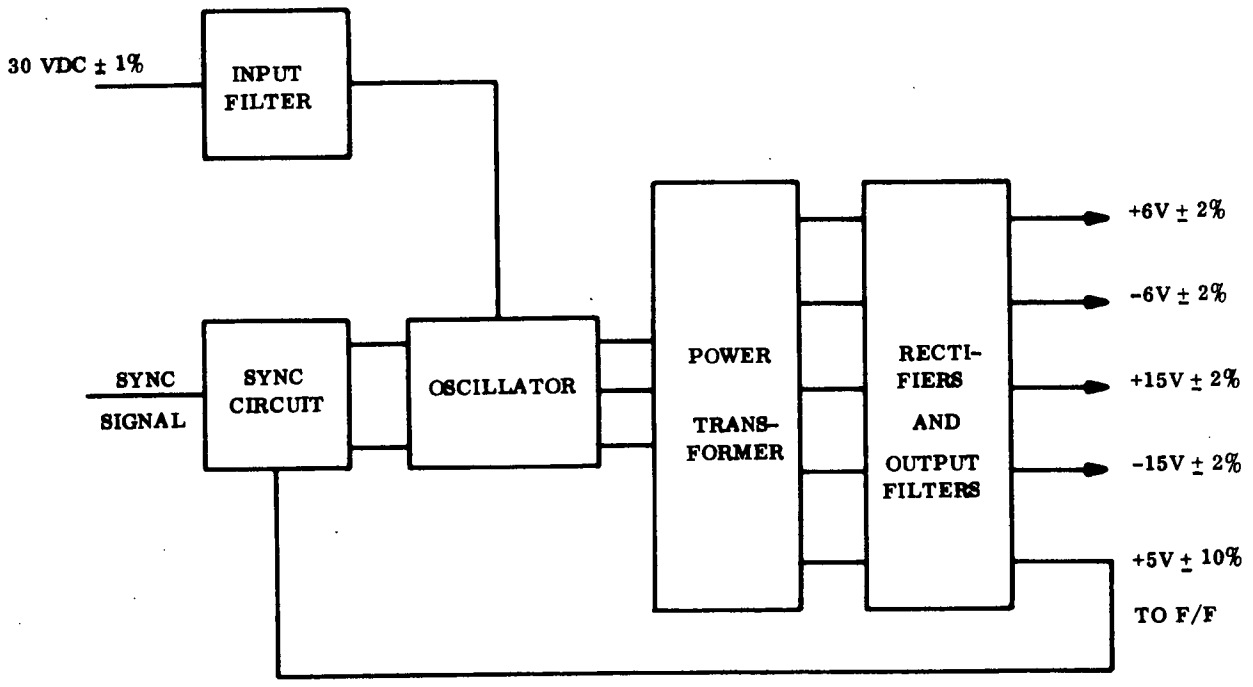
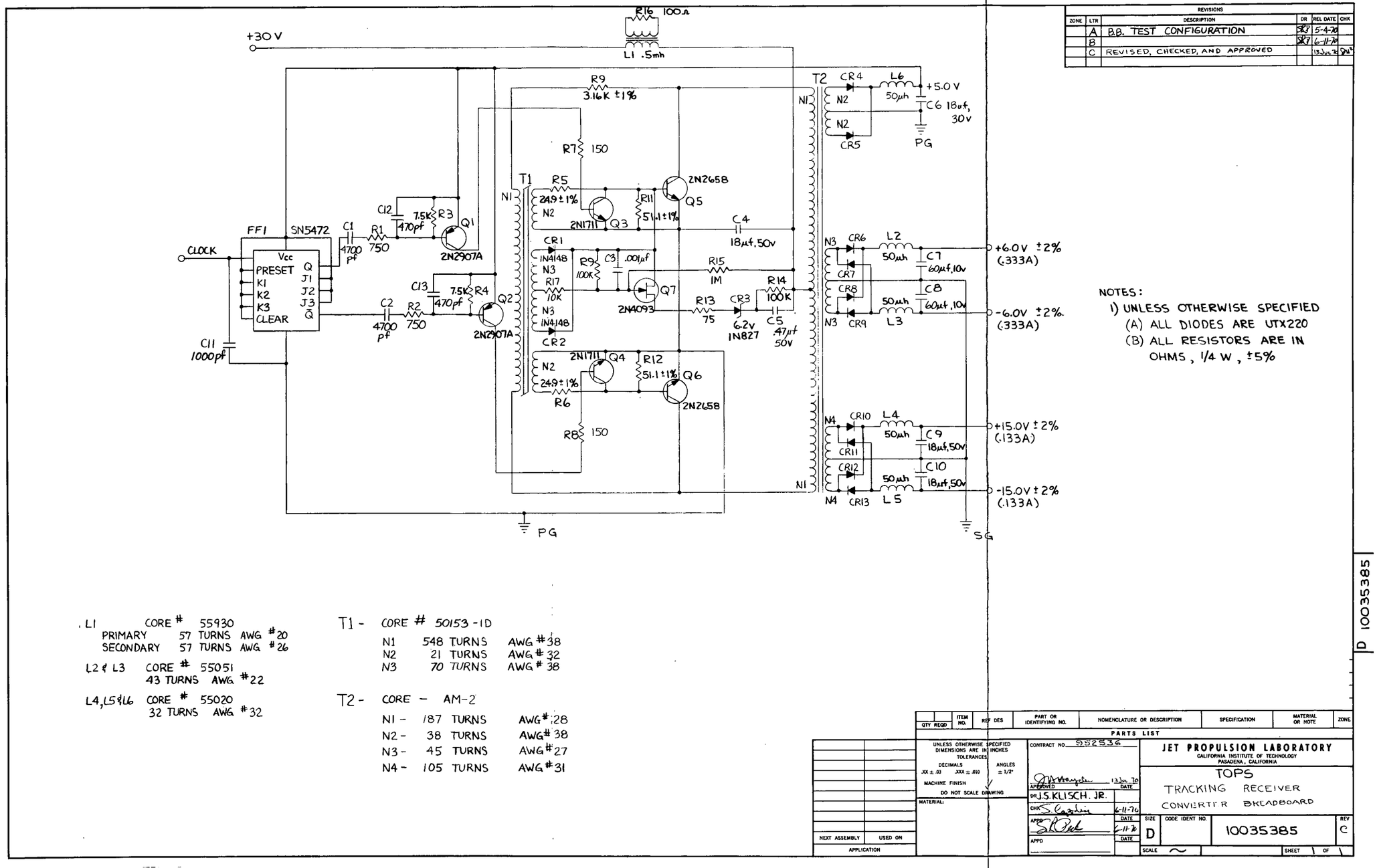


Figure 6.3-4. Tracking Receiver Converter Block Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2



NOTES:

1) UNLESS OTHERWISE SPECIFIED
   (A) ALL DIODES ARE UTX220
   (B) ALL RESISTORS ARE IN OHMS, 1/4 W, ±5%

L1 CORE # 55930
PRIMARY 57 TURNS AWG #20
SECONDARY 57 TURNS AWG #26

L2 & L3 CORE # 55051
43 TURNS AWG #22

L4, L5 & L6 CORE # 55020
32 TURNS AWG #32

T1 - CORE # 50153-1D
N1 548 TURNS AWG #38
N2 21 TURNS AWG #32
N3 70 TURNS AWG #38

T2 - CORE - AM-2
N1 - 187 TURNS AWG #28
N2 - 38 TURNS AWG #38
N3 - 45 TURNS AWG #27
N4 - 105 TURNS AWG #31

REVISIONS					
ZONE	LTR	DESCRIPTION	DR	REL DATE	CHK
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	B		JKT	6-11-76	
	C	REVISED, CHECKED, AND APPROVED		13 JUL 76	DM

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PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010
ANGLES ± 1/2°
MACHINE FINISH
DO NOT SCALE DRAWING
MATERIAL:

NEXT ASSEMBLY | USED ON
APPLICATION

CONTRACT NO. 952536

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

TOPS
TRACKING RECEIVER
CONVERTER BREADBOARD

APPROVED		13 JUL 76	DATE
DR	J.S. KLISCH, JR.		
CHK		6-11-76	DATE
APPD		6-11-76	DATE
APPD			DATE

SIZE	CODE IDENT NO.		REV
D		10035385	C

SCALE ~ SHEET \ OF \

D 10035385

Figure 6.3-5. Tracking Receiver Converter Breadboard Schematic

6.3.3 DC MAGNETOMETER CONVERTER

The DC Magnetometer Converter provides six regulated outputs as specified in Table 6.3-3. The outputs are required to stay within the regulation limits over variations in line (30 vdc ± 1%) and temperature (0°C to 40°C), and the converter is required to withstand and recover from temperature extremes of -20°C and +80°C. The converter has the capability of operating in either a free-running mode or in a clock driven mode. A block diagram is shown on Figure 6.3-6; an electrical schematic is shown on Figure 6.3-7. Two types of dissipative regulators are provided: one with discrete piece parts for the 24 volt supply and one with operational amplifiers for the 5-volt supplies. In other respects, the converter is identical to that described for the Science Data Subsystem (para. 6.3.1).

Table 6.3-3. Output Requirements of the DC Magnetometer Converter

Output Voltage (Volts)	Regulation (percent)	Load Current (ma)	Load Power (watts)
+24.0	± 0.5	50	1.200
+ 5.0	± 5.0	125	0.625
+ 5.0	± 0.1	5	0.025
- 5.0	± 0.1	5	0.025
+12.0	± 5.0	50	0.600
-12.0	± 5.0	50	0.600

6.3.4 PACKAGING CONSIDERATIONS

One of the efforts covering dc to dc converter design was to examine the possibility of standardizing certain circuit elements as a step toward improved packaging and cost. The results of this effort are described below.

The piece part density of space power conditioning equipment has not kept pace with improvements in other subsystems. The non-uniform sizes and shapes of the mechanical devices and the electronic piece parts have not lent themselves to efficient packaging.

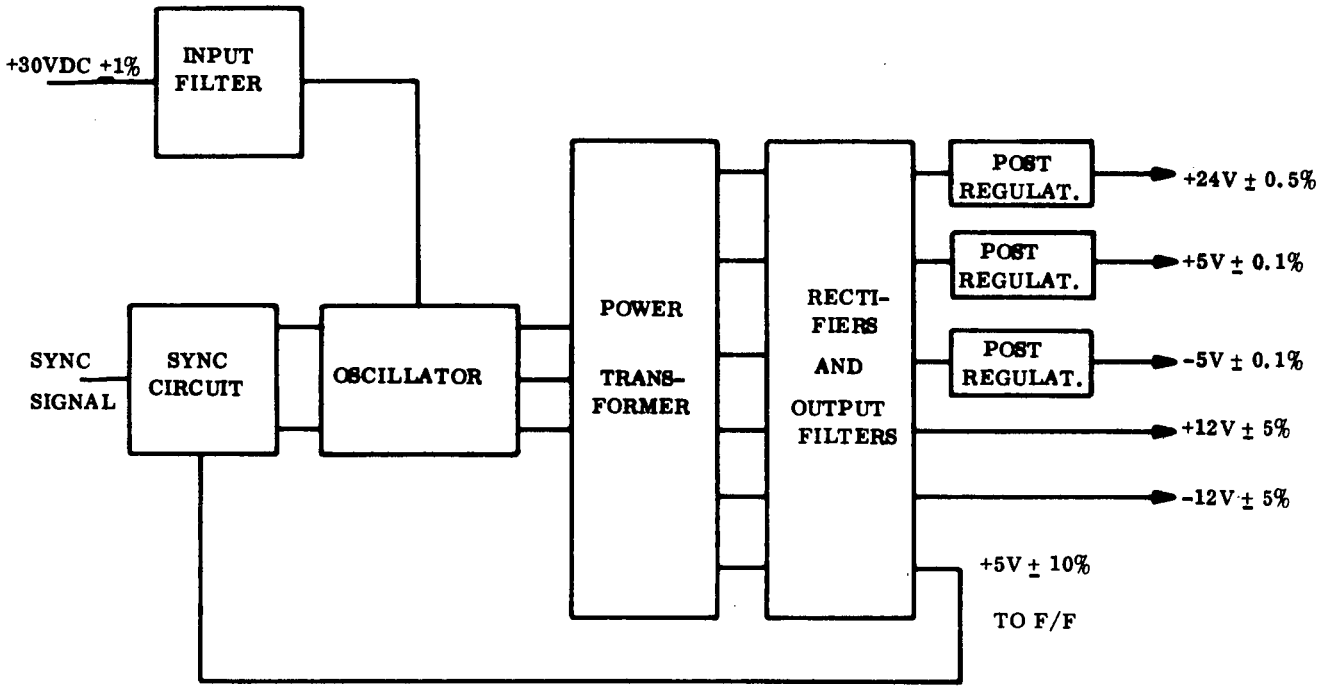

Figure 6.3-6. DC Magnetometer Converter Block Diagram

Design improvements are being developed by applying thin and thick film microcircuit techniques to power equipment. This has occurred only in the past few years, even though these techniques have been applied in other areas for 10 years. This delay is due to the small degree of standardization and the high thermal density that occurs when high power piece parts are put into small volumes.

A task of the TOPS power conditioning equipment study was to develop a hybrid thick film microcircuit of the electronic parts of a dc to dc converter. This one basic, multipurpose circuit can be used to satisfy 35 separate requirements on the TOPS project with conditioned power levels from 1 to 25 watts. Three models have been identified for this range of power and all 3 can be built on the same conductor layout, with variations in the values of 7 piece parts only.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

10035387

REVISIONS					
ZONE	LTR	DESCRIPTION	DR	REL DATE	CHK
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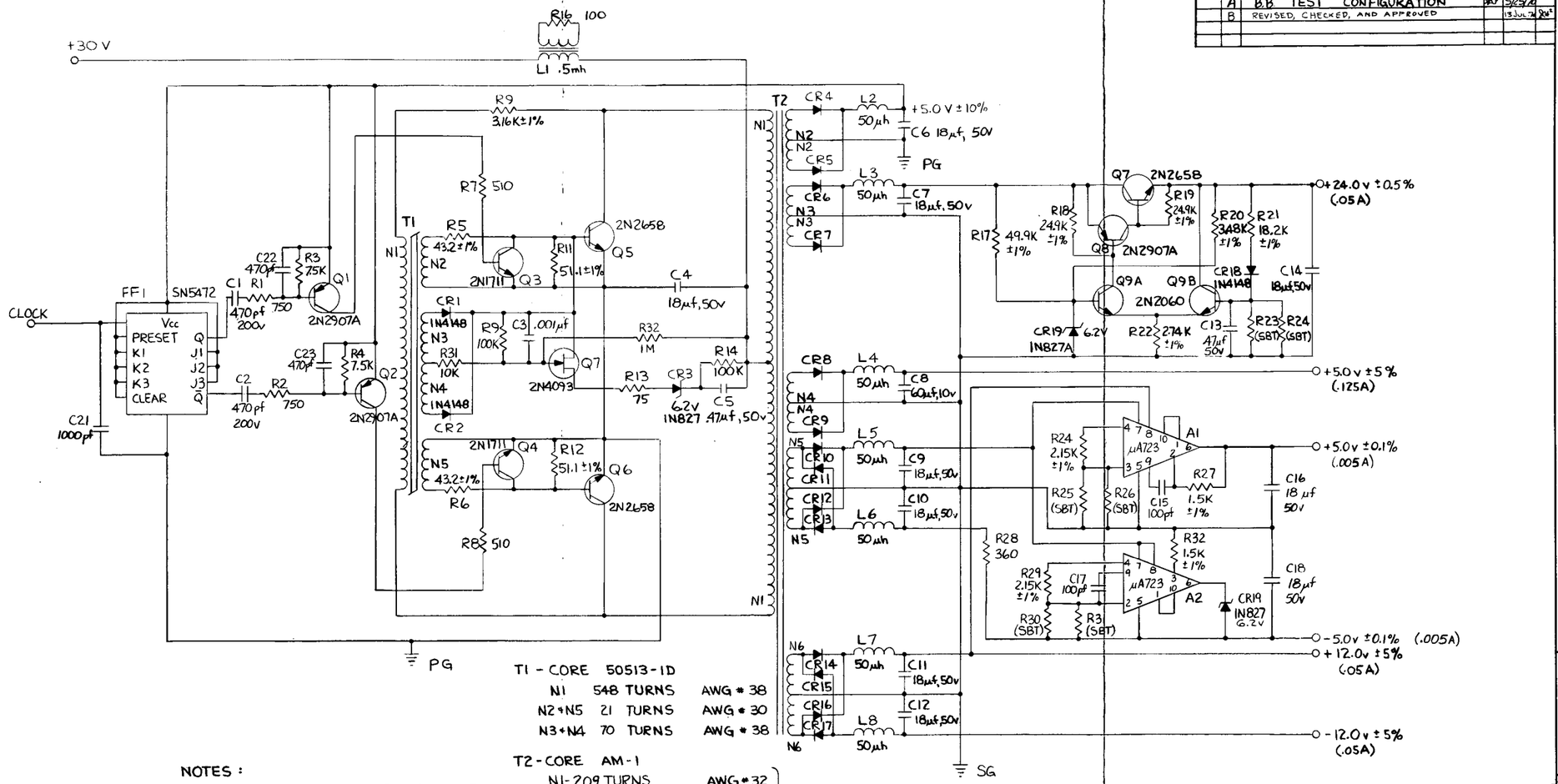
	B	REVISED, CHECKED, AND APPROVED		13 JUL 72	JKP



T1 - CORE 50513-1D

N1	548 TURNS	AWG # 38
N2+N5	21 TURNS	AWG # 30
N3+N4	70 TURNS	AWG # 38

T2 - CORE AM-1

N1	209 TURNS	AWG #32
N2	45 TURNS	AWG #38
N3	203 TURNS	AWG #35
N4	43 TURNS	AWG #30
N5	66 TURNS	AWG #38
N6	95 TURNS	AWG #33

BIFILAR WOUND

L1 - CORE 55930

PRIMARY 57 TURNS AWG #20
SECONDARY 57 TURNS AWG #26

L2 THRU L8 CORE 55020
32 TURNS AWG #32

NOTES:
1) UNLESS OTHERWISE SPECIFIED
(A) ALL DIODES ARE UTX220
(B) ALL RESISTORS ARE IN OHMS, 1/4 W, ±5%

QTY REQD	ITEM NO.	REF DES	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	MATERIAL OR NOTE	ZONE

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX ± .03 .XXX ± .010
ANGLES ± 1/2°
MACHINE FINISH
DO NOT SCALE DRAWING
MATERIAL:

CONTRACT NO. 952536

APPROVED		DATE 13 Jul '72
DR J.S. KLISCH, JR		DATE 15 Mar '72
CHK S. Peck		DATE 5-24-72
APPD S. Logan		DATE 5-24-72
APPD		DATE

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA

TOPS
DC MAGNETOMETER CONVERTER
BREADBOARD

SIZE	CODE IDENT NO.		REV
D		10035387	B

SCALE SHEET 1 OF 1

NEXT ASSEMBLY USED ON
APPLICATION

D 10035387

Figure 6.3-7. DC Magnetometer Converter Breadboard Schematic

The inherent physical properties of the flat pack materials and construction enhances heat transfer, and balances the increased thermal density with higher conductivity and shorter thermal paths. Figure 6.3-8 is a scale layout of the parts within the flat pack with piece part designation, and Figure 6.3-9 is a photographic reproduction of the actual circuit.

The aluminum oxide substrate, which is the means by which the circuit conductor and electronic piece parts are held within the flat pack, has a very high thermal conductivity and is an excellent electrical insulator. This property provides a more direct and efficient path of heat flow from the internally mounted switching power chips and the other internally mounted dissipative elements to the bottom of the metal flat pack. The flat pack in turn is then mounted or bonded to a metal heat sink with either a highly heat conductive paste, or a low temperature solder. This small number of highly efficient thermal interfaces provides excellent heat transfer. This can be compared to a semi-conductor chip that is mounted in an ordinary transistor case and insulated from the metal heat sink for electrical integrity. It uses a mechanical screw or nut for mounting, producing a higher thermal resistance to the ultimate heat sink. The flat pack itself is rated at 25 watts per square inch of mounting surface. This assumes that it is bonded to a heat sink which will adequately remove this much power.

Under normal discrete part construction of a dc to dc converter, the electrical (non-magnetic) piece parts are mounted on a printed circuit board or in a cordwood module. Either of these concepts would need additional means of heat transfer to maintain the piece parts at allowable temperatures. Further, the spacing of the discrete piece part under construction creates longer interconnections, higher power dissipation in the additional wire and increased opportunity for noise coupling into adjacent circuitry.

A comparison of flat pack and discrete piece part packaging indicates a weight reduction of 80 percent, a volume reduction of 80 percent, and a reduction in the number of interconnections from 44 to 13 (see Table 6.3-4).

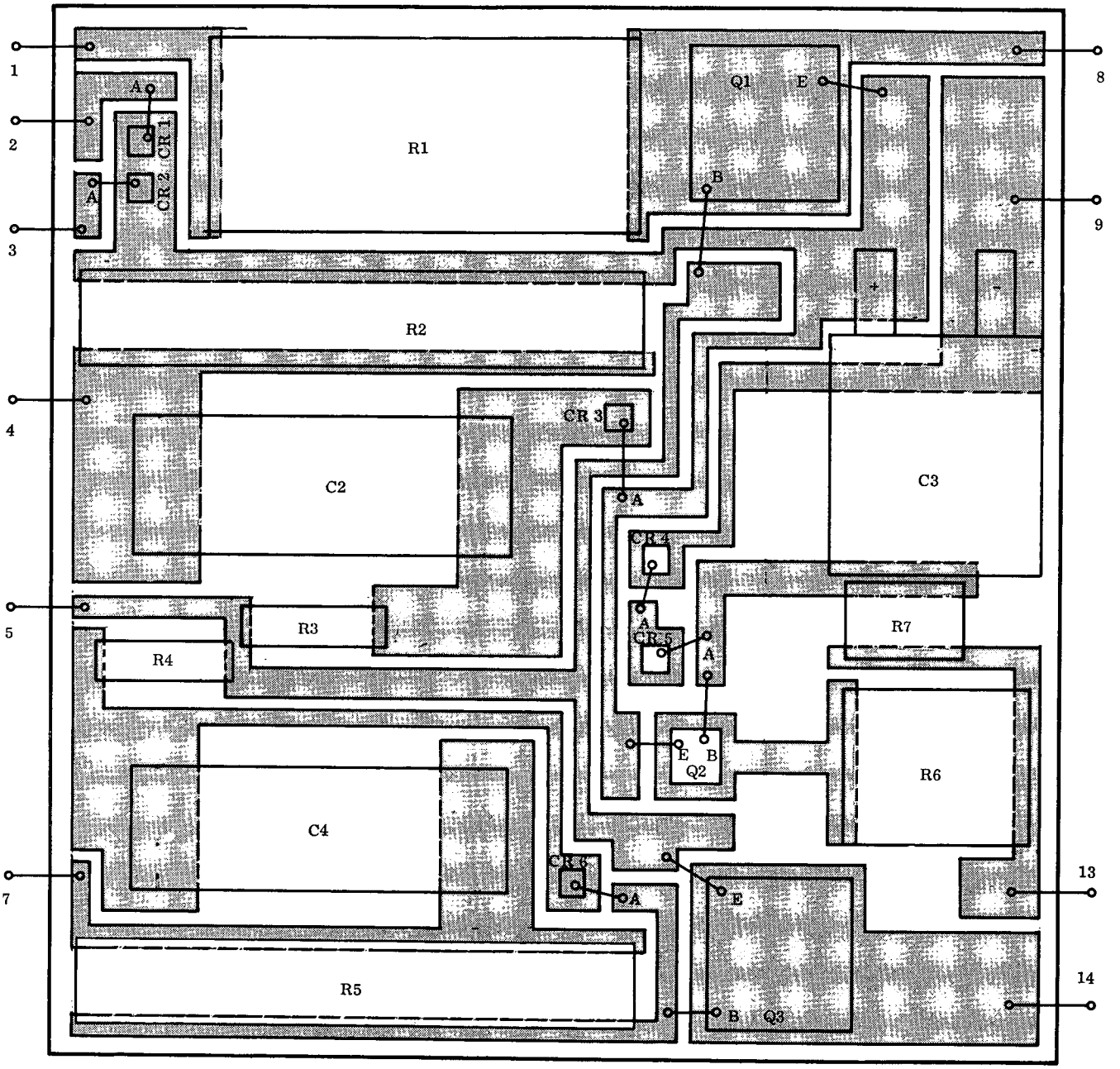


Figure 6.3-8. Thick Film Microcircuit Physical Layout

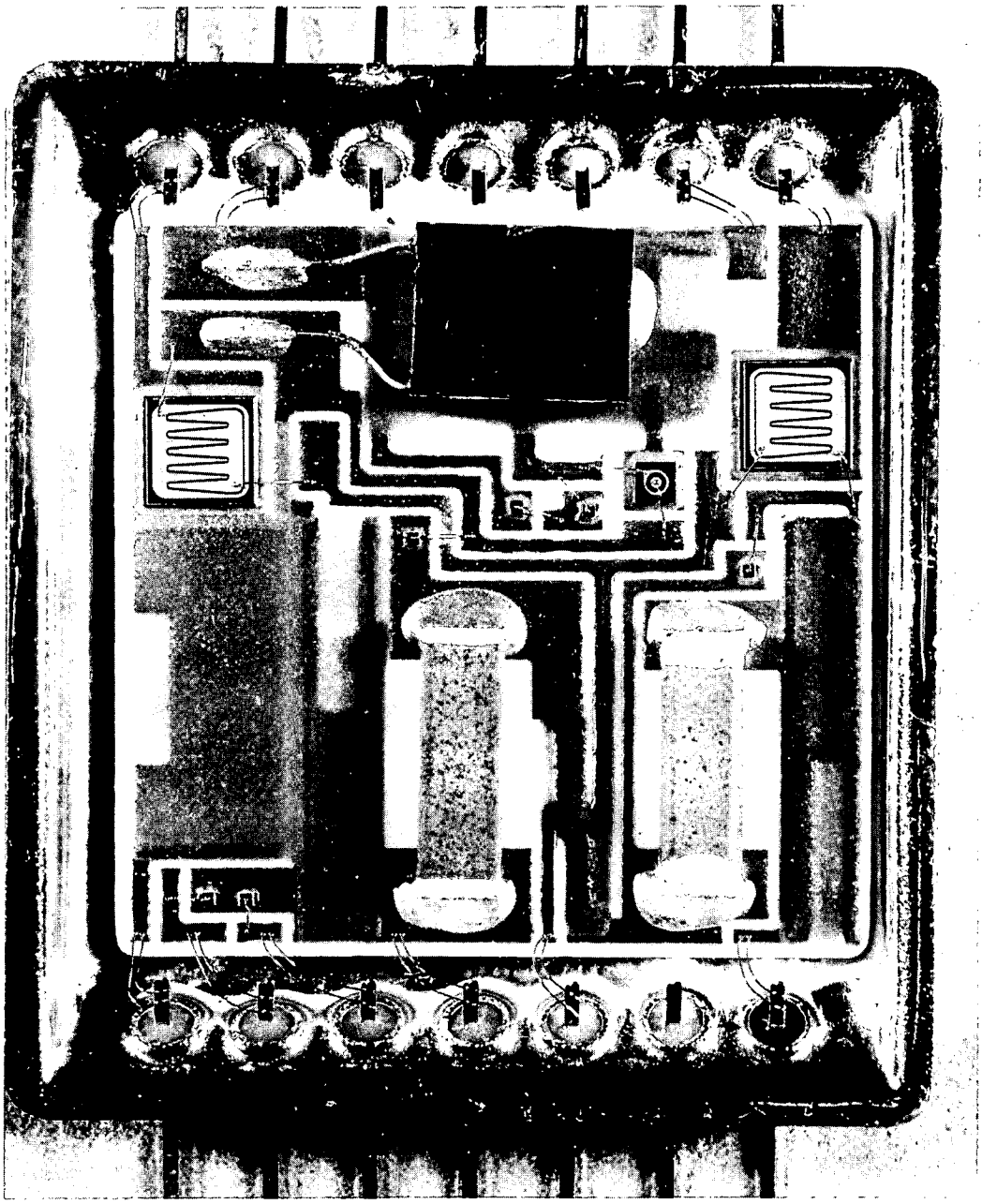


Figure 6.3-9. Thick Film Microcircuit

Table 6.3-4. Weight Comparison of Discrete Parts versus Flatpack

Weight of Discrete Parts (pounds)		Weight of Flatpack (pounds)
R1	0.003	0.0125
R2	0.001	
R3	0.001	
R4	0.001	
R5	0.001	
R6	0.001	
R7	0.001	
CR1	0.0005	
CR2	0.0005	
CR3	0.0005	
CR4	0.0005	
CR5	0.0005	
CR6	0.0005	
C2	0.002	
C3	0.005	
C4	0.002	
Q1	0.007	
Q2	0.007	
Q3	0.007	
Printed Circuit Board	0.020	
	0.062	0.0125

SECTION 7
CONCLUSIONS

This program was concerned with analysis of system requirements, configuration studies to determine the optimum arrangement of equipment, and the development of circuits and devices to meet the extended life requirement of an outer planet mission. The principal conclusions of the program are that no severe technological problems associated with extended life capability have been encountered, and circuit redundancy techniques are practical and have been applied successfully to solid-state and relay switching devices and to the shunt regulator.

Alternative shunt regulator concepts were examined in consideration of the dissipation that can be accepted by the PCE bay, and based on this thermal burden limitation, a sequence shunt appears to offer the most suitable characteristics.

Long term flight batteries for a TOPS Spacecraft appear neither necessary nor desirable. The prinicpal benefit of batteries would be to reduce turn-on voltage transients. It is considered that other less complex techniques can be used to relieve such transients. Additionally, the weight penalty of battery averaging is at least four times as great as increasing the RTG size to provide direct power, thus the use of batteries for power averaging does not appear to be justified.

Launch batteries to augment limited on-pad RTG capability were evaluated. As a result of the complexity introduced, their use is not recommended. Provisions for on-pad power capability have been implemented into the RTG design.

The most radiation sensitive transistor in the circuits under consideration is the high voltage series regulator pass transistor in the traveling wave tube converter. This selection was made on the premise that the results of increased leakage current could not be compensated for easily by device selection or device change. The results of radiation testing, however, demonstrated that the open emitter leakage current did not increase significantly

and that the gain degradation actually caused a decrease in the open base leakage current. The conclusion is that radiation sensitivity of all electrical piece parts must be considered carefully, but that adequate designs could survive the expected radiation.

Emphasis has been placed on ac power distribution as a result of a JPL project decision. A power busing concept was developed which provides a Main Bus and a Protected Bus. The Fault Detection and Correction (FD&C) equipment use the Protected Bus as their prime source of power and the Main Bus as a back-up source. All other spacecraft equipment operate from the Main Bus exclusively. Development of a Protected Bus insensitive to faults on the Main Bus was accomplished by the use of a current throttle concept which isolates one RTG from the common Main Bus during fault condition periods.

It is not possible to communicate with the spacecraft without the inverter which provides ac power to the Radio Frequency Subsystem. Therefore, dedicated failure detection was selected for the inverters to maximize reliability.

To back-up the Fault Detection and Correction equipment to protect against a long duration main bus undervoltage condition, a Low Voltage Cut Off circuit was included in the Power Conditioning Equipment. This simple non-redundant device removes spacecraft loads if the Main Bus voltage goes out of specification for a period far exceeding the time required for correction by the normal FD&C method.

Breadboard circuits were developed and tested over the required temperature range for each function of the Power Conditioning Equipment. These operational circuits provided the basis then for a thorough reliability study. Through the use of active and standby redundancy techniques, the probability that the Power Subsystem will provide all its functions to the spacecraft at end of mission was found to be 97 percent.

SECTION 8
RECOMMENDATIONS

The following recommendations are based on the results of this program. In general, the recommendations address effort improve and further develop the baseline design of the Power Subsystem described in this report.

With respect to the Power Subsystem configuration, the following activities are recommended:

1. The reliability study of the baseline quad redundant shunt regulator suggested that higher reliability could be obtained with fewer piece-parts by rearrangement of elements. This concept should be developed.

2. All power to the Main Bus passes through the RTG isolation diodes. A significant quantity of power (16 watts EOM) is unavailable for use by the spacecraft loads due to the loss in these diodes. An in-depth failure modes and effects analysis should be performed on the RTG to determine the probability that single internal failures would load down the remaining RTGs of the Power Subsystem. A low degree of probability could result in elimination of the isolation diodes.

3. The concepts of load fault detection and correction is highly dependent on the CCS interface to the power distribution switches. The Remote Decoder Array interface should be developed to the same depth as the other segments of the Power Conditioning Equipment.

4. The Power Subsystem is highly redundant by necessity. A study should be conducted to determine how this redundancy will be verified during all levels of Power Subsystem testing. The results of such a study would probably require design modifications to the present circuitry to provide test capability.

5. Studies show that a higher system reliability can be obtained by reconfiguring the interface between the command generators of the Inverter Failure Detector and the Inverter Switches. (Reference Section 3.6.3.) This change is recommended.

For the circuitry described in Section 5 of this report, the following design changes should be made prior to a flight application:

1. Current Throttle

Due to the reduction in current through the by-pass circuit, the Darlington transistor arrangement of Q4-Q5 can most likely be eliminated. A single transistor will suffice. The operational amplifier should be changed from an LM208 to an LM101A to survive a possible Main Bus high voltage transient condition.

2. Current Throttle Steering Switch

The energy storage capacitor C3 should be increased by 20 percent to increase the margin of the switch power duration. Higher voltage transistors should be used to withstand the RTG open circuit voltage.

3. Shunt Regulator

A single failure in the control circuit of either lower segment of the quad shunt regulator can cause a continuous power drain of as much as 50 watts from the Main Bus. This failure mode should be eliminated.

4. Main Inverter

The Main and Protected Buses should be ordered together at the input of the current limit circuitry to protect the transistors in the multivibrator during an under-voltage condition.

5. Inverter Switch

The 2N2222A transistors should be replaced with a type with a V_{CEO} of 60 vdc or higher to protect against transient conditions which could cause overvoltage breakdown.

6. Inverter Failure Detector and Switch Command Generator

The discharge time of the inverter failure detector capacitor C7 must be shortened such that the failure signal stops approximately one millisecond or less after the input signals to the failure detector return to normal and indicates that the inverter is operating properly.

Also, the 2N2222A transistors should be replaced to protect against transient conditions which could cause overvoltage breakdown.

7. Power Distribution Switch

The 2N2222A transistors should be replaced with a type with a V_{CEO} of 60 vdc or higher to protect against transient conditions which could cause overvoltage breakdown.

8. Low Voltage Cut Off

The 2N2222A transistors should be replaced with a type with a V_{CEO} of 60 vdc or higher to protect against transient conditions which could cause overvoltage breakdown.

SECTION 9
NEW TECHNOLOGY

The following are identified as new technology items which were developed under this contract.

I
- DC to AC Inverter Ratio Failure Detector
- T. J. Ebersole and R. E. Andrews
- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Final Report 72SD4223, Sections 4.4.2.2 and 5.8, June 15, 1972.

II
- Redundant Power Distribution Switch
- T. J. Ebersole and J. Klisch
- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Final Report 1J86-TOPS-940, Sections 4.3 and 5.9, May 19, 1972.

III
- Sequenced Shunt Regulator
- A. Kirpich and J. H. Hayden
- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Final Report 1J86-TOPS-940, Sections 4.2.2 and 5.3, May 19, 1972.

IV
- Protected Bus Concept
- A. Kirpich and R. E. Andrews
- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Technical Report for First and Second Quarters, 1970. 1J86-TOPS-650, Section 3.3.3.3, August 1, 1970.
- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Final Report 1J86-TOPS-940, Sections 4.3, 4.3.3, 4.4.1, 4.5.2, 5.1 and 5.2.

V
- High Voltage Regulator Using Low Voltage Transistors
- J. H. Hayden and R. Andryczyk
- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Quarterly Technical Report for Fourth Quarter, 1969. 1J86-TOPS-513 Section - Appendix I February 15, 1970.

- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Quarterly Technical Report for Third Quarter, 1970. 1J86-TOPS-650 Section - Appendix F October 15, 1970.

- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Final Report 72SD4223 Section 6.1, June 15, 1972.

VI
- Redundant Regulator Control with Low Standby Losses

- R. Andryczyk and S. Peck

- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Final Report 1J86-TOPS-940 Section 4.2.2 and 5.2, May 19, 1972.

VII
- Forced Start Converter Circuit

- R. Andryczyk and S. Capodici

- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Quarterly Technical Report for Third Quarter, 1970. 1J86-TOPS-650 Section - Appendix F October 15, 1970.

VIII
- Hybrid Thick Film Microcircuit for Converter Electronics

- S. Capodici and S. Peck

- Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft, Quarterly Technical Report for Fourth Quarter, 1969. 1J86-TOPS-513 Section - Appendix K February 15, 1970.

SECTION 10
REFERENCES AND BIBLIOGRAPHY

1J86-TOPS-479 Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft Power Subsystem, Quarterly Technical Report, 15 October 1969.

1J86-TOPS-480 Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft Power Subsystem, Quarterly Technical Report, 15 December 1969.

1J86-TOPS-513 Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft Power Subsystem, Quarterly Technical Report, 15 February 1970.

1J86-TOPS-555 Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft Power Subsystem, Technical Report for First and Second Quarters, 1970; 1 August 1970.

1J86-TOPS-650 Power Conditioning Equipment for a Thermoelectric Outer Planet Spacecraft Power Subsystem, Technical Report for Third Quarter, 1970; 15 October 1970.

APPENDIX A
RELIABILITY ANALYSIS

Enclosed herein are the data and programs used in determining the Power Subsystem reliability.

Table A-1 contains the High and Low piece part failure rates used in the circuit analysis.

Table A-2 is a summary of the number of piece parts used for each circuit type and their contribution to failures open and failures short. The high failure rates of Table A-1 are used.

Table A-3 is the same as Table A-2 but uses the low failure rates.

Table A-4 is the computer program developed to determine Shunt Regulator Reliability.

Tables A-5, A-6, A-7, and A-8 are printouts of the Shunt Regulator program which were used in the construction of Figure 4.5-17 in the text.

Table A-9 explains the Markov Chain analysis used for those subsystem functions that involve switching out failed units and switching in standby units.

Table A-10 contains the detailed reliability equations for the Current Throttle/Steering Switch.

Table A-11 presents the reliability equations for the Inverter.

Tables A-12 and A-13 are printouts of the computer programs for calculating inverter reliability.

Table A-14 is the computer program developed to determine overall Power Subsystem reliability.

Table A-1. Piece-Part Failure Rates

Part	High Failure Rate (x 10^{-6} Failures/Hour)	Low Failure Rate (x 10^{-6} Failures/Hour)
Capacitor - Tantalum	0.01	0.006
Ceramic	0.005	-
Mica	-	0.002
Diode - Signal	0.01	0.002
Zener	0.02	0.005
Power	0.05	0.008
Resistor - Metal Film	0.008	0.002
Carbon Composition	0.001	0.003
Power	0.09	0.03
Wire Wound	0.09	0.02
Transistor-FET	0.02	0.003
Signal	0.02	0.003
Power	0.08	0.01
Op Amp - Bipolar	0.2	0.09
Magnetic Amplifier	0.018	0.003
Power Transformer	0.018 per winding	0.003 per winding
Transformer	0.006 per winding	0.001 per winding
Choke	0.01	0.001
Relay	2.0	0.5

FOLDOUT FRAME 1

FOLDOUT FRAME 2

FOLDOUT FRAME 3

Table A-2. Component Summary
High Failure Rates

Component		Relay Driver			Failure Detector			Command General			Inverter			Current Throttle			CT Steering Switch Detector			CT Relay Driver			Shunt Regulator Electronics													
																							Drive			Sequence #1			Sequence #2			Sequence #3			Sequence #4		
Part	λ	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S
Capacitor - Tant	.01				(1)	.005		(1)	.005		2	.02		1		.005	(3)	.015	.015																	
- Ceramic	.005				3	.005	.010				8	.04		1	.0025	.0025							1	.0025	.0025											
- Mica																																				
Diode - Signal	.01	(2)	.01		16	.12	.04	1	.01		10	.10					1	.01		1	.005	.005														
	.02				2	.02	.02	(1)	.01		2	.04		(3)	.03	.03	3	.03	.03				1	.01	.01				2	.04		1	.02		1	.02	
- Power	.05										4	.20																							
Resistor - Met Film	.008				21	.096	.072	2	.008	.008	4	.032		4	.008	.024	8	.04	.024				8	.032	.032	3	.008	.016	3	.008	.016	3	.008	.016	3	.008	.016
- Carbon C.	.001	6	.003	.003	4	.002	.002				22	.022		7	.003	.004	5	.0035	.0015	3	.001	.002														
- Power	.09										3	.27		2	.09	.09									2	.18		2	.18		2	.18		2	.18	
- Wire Wound	.09																								3*	.016875	.016875	2*	.01125	.01125	2*	.01125	.01125	2*	.01125	.01125
Transistor - FET	.02																																			
- Signal	.02	3	.03	.03	2	.02	.02	1	.01	.01	2	.04		1	.01	.01	2	.02	.02	2	.02	.02	1	.01	.01											
- Power	.08										5	.40		4	.16	.16							1	.04	.04	4	.16	.16	3	.12	.12	3	.12	.12	3	.12	.12
Op Amp - Bipolar	.2				2	.2	.2				1	.20		1	.10	.10	1	.10	.10				1	.1	.1											
Mag Amp	.018				1	.018																														
Power Transformer	.018/wdg										7	.126																								
Transformer	.006/wdg				8	.018	.030				6	.036																								
Choke	.01										2	.02																								
Relay	2.0																																			
Total λ		.076			.898			.056 (Quad) .061 (Present)			1.546			.834			.409			.053			.389			.55775			.5065			.4865			.4865		
% Open		.566			.561			.679 (Quad) .705 (Present)						.490			.534			.491			.500			.654			.709			.697			.697		

NOTES: 1. ALL FAILURE RATES ARE FAILURES PER MILLION HOURS

2. PARENTHESIS INDICATES THAT MORE PARTS EXIST IN THE CIRCUITRY, BUT DO NOT CONTRIBUTE TO UNRELIABILITY.

*SHOWN DERATED TO .01125 DUE TO APPLICATION

A-3.1

A-3

FOLDOUT FRAME 1

FOLDOUT FRAME 2

FOLDOUT FRAME 3

Table A-3. Component Summary
Low Failure Rates

Component		Relay Driver			Failure Detector			Inverter					Current Throttle			CT Steering Switch Detector			CT Relay Driver			Shunt Regulator Electronics													
																						Drive			Sequence #1			Sequence #2			Sequence #3			Sequence #4		
Part	λ	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O		#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S	#	λ_O	λ_S
Capacitor - Tant	.006				(1)	.003		(1)	.003	2	.012		1		.006	(3)	.012	.012																	
- Ceramic																																			
- Mica	.002				3	.002	.004			8	.016		1	.001	.001							1	.001	.001											
Diode - Signal	.002	(2)	.002		16	.024	.008	(1)	.001	10	.020					1	.002		1	.01	.01														
- Zener	.005				2	.005	.005	(1)	.0025	2	.010		(3)	.0075	.0075	3	.0075	.0075				1	.0025	.0025				2	.01		1	.005		1	.005	
- Power	.008									4	.032																								
Resistor - Met Film	.002				21	.024	.018	2	.002	4	.008		4	.002	.006	8	.010	.006				8	.008	.008	3	.002	.004	3	.002	.004	3	.002	.004	3	.002	.004
- Carbon C.	.0003	6	.0009	.0009	4	.0006	.0006			22	.0066		7	.0009	.0012	5	.00105	.00045	3	.0003	.0006														
- Power	.03									3	.09		2	.03	.03										2	.06		2	.06		2	.06		2	.06	
- Wire Wound	.02																								3*	.00375	.00375	2*	.0025	.0025	2*	.0025	.0025	2*	.0025	.0025
Transistor - FET	.003																																		
- Signal	.003	3	.0045	.0045	2	.003	.003	1	.0015	2	.006		1	.0015	.0015	2	.003	.003	2	.003	.003	1	.0015	.0015												
- Power	.01									5	.05		4	.02	.02							1	.005	.005	4	.02	.02	3	.015	.015	3	.015	.015	3	.015	.015
Op Amp - Bipolar	.09				2	.09	.09			1	.09		1	.045	.045	1	.045	.045				1	.045	.045												
Mag Amp	.003				1	.003																													
Power Transformer	.003/wdg									7	.021																								
Transformer	.001/wdg				8wdg	.009	.015			6	.006																								
Choke	.001									2	.002																								
Relay	.5																																		
Total λ			.0128			.3072			.0135 (Quad) .0165 (Present)		.3696			.2261			.1545			.0089			.126			.1135			.111			.106			.106	
% Open			.578			.533			.741 (Quad) .788 (Present)					.477			.521			.483			.500			.756			.806			.797			.797	

*SHOWN DERATED TO .0025 DUE TO APPLICATION

NOTES: 1. ALL FAILURE RATES ARE FAILURES PER MILLION HOURS

2. PARENTHESIS INDICATES THAT MORE PARTS EXIST IN THE CIRCUITRY, BUT DO NOT CONTRIBUTE TO UNRELIABILITY.

A-5

A-5.1

Table A-4. Shunt Regulator Reliability Program

* * * *

FILE SREL-71 LISTING 12/16/71 11.163 PAGE 01

```
00010 DIMENSION NRES(4),NFRES(10,4),RBANK(4)
00020 DOUBLE PRECISION RRES,YRES,X,QRES,PRS,PO,PS,R1,R2,R3,R4,
00030 &Y1,Y2,Y3,Y4,PO1,PO2,PO3,PO4,PS1,PS2,PS3,PS4,YD,RD,POD,PSD,
 00040 &RELECT,T,XT,YO1,YO2,YO3,YO4,PPO,PPS,PSS,PGG,FACT,SUM,XFACT,
 00050 &RSHUNT,RBANK,RQ1,RQ2,RQ3,RQ4,YCAP,RCAP,RCAPB,FACTCAP
00060 PRINT:"LAMBDAS-FAILURES/MILLION HOURS"
00070 PRINT:" ELECTRONICS DATA-LAMBDA,% OPEN-DRIVE,STRINGS-1,2,3,4"
 00080 PRINT:" " ; READ:YD,YOD,Y1,YO1,Y2,YO2,Y3,YO3,Y4,YO4
00090 PRINT:" POWER RESISTOR LAMBDA.%OPEN" ; READ:YRES,YORES
00100 PRINT:" BANK DATA-# PARALLEL STRINGS/BANK-1,2,3,4"
00110 READ:(NRES(I),I=1,4)
00120 PRINT:" CAPACITOR BANK-LAMBDA,# CAPS,# ALLOWED TO FAIL"
00130 READ:YCAP,NCAP,NFCAP
00140 PRINT:" TIMES(YEARS)-START,STOP,# PRINTOUTS" ; READ:T1,T2,NIT
 00150 DELT=(T2-T1)/(NIT-1) ; TX=T1-DELT
00160 *****  RESISTOR BANKS *****
00170 PRINT:" TIME(YEARS):ALLOWED FAILURES-BANK"
00180 PRINT 1003
00190 DO 100 I=1,NIT
00200 TX=TX+DELT ; PRINT 1001,TX
00210 100 READ:(NFRES(I,J),J=1,4)
00220 TX=T1-DELT
00230 PRINT:" TIME   SHUNT REL"
00240 PRINT:"          RE      RCAPS        RB1        RB2        RB3
 00250 &        RB4"
00260 DO 101 I=1,NIT
00270 TX=TX+DELT
00280 T=TX*365.25*24/1000000
00290 RRES=DEXP(-T*YRES) ; PRS=(1-YORES)*(1.-RRES)
00300 RRES=RRES*RRES+2.*RRES*PRS
```

* * * *

Table A-4. Shunt Regulator Reliability Program (Cont'd)

* * * *

FILE SREL-71 LISTING 12/16/71 11.163 PAGE 02

```
00310 QRES=1.-RRES-PRS*PRS
00320 DO 121 K=1,4
00330 SUM=RRES**NRES(K)  ;  FACT=1.
00340 KN=NFRES(I,K)
00350 IF(KN.EQ.0)GO TO 121
00360 DO 122 KK=1,KN
00370 XFACT=(NRES(K)+1-KK)/KK
00380 FACT=FACT*XFACT
00390 122 SUM=SUM+FACT*RRES**(NRES(K)-KK)*QRES**KK
00400 121 RBANK(K)=SUM
00410 ***** ELECTRONICS*****
00420 R1=DEXP(-T*Y1)
00430 P01=Y01*(1.-R1) ; PS1=(1-Y01)*(1.-R1)
00440 RQ1=1-(2*P01*P01-P01**4+4*PS1*PS1-4*PS1**3+PS1**4)
00450 R2=DEXP(-T*Y2) ; P02=Y02*(1-R2) ; PS2=(1-Y02)*(1-R2)
00460 RQ2=1-(2*P02*P02-P02**4+4*PS2*PS2-4*PS2**3+PS2**4)
00470 R3=DEXP(-T*Y3) ; P03=Y03*(1-R3) ; PS3=(1-Y03)*(1-R3)
00480 RQ3=1-(2*P03*P03-P03**4+4*PS3*PS3-4*PS3**3+PS2**4)
00490 R4=DEXP(-T*Y4) ; P04=Y04*(1-R4) ; PS4=(1-Y04)*(1-R4)
00500 RQ4=1-(2*P04*P04-P04**4+4*PS4*PS4-4*PS4**3+PS4**4)
00510 RD=DEXP(-T*YD) ; POD=Y0D*(1-RD) ; PSD=(1-Y0D)*(1-RD)
00520 PGG=RD*R1*R2*R3*R4
00530 PPO=POD*(1-PS1)*(1-PS2)*(1-PS3)*(1-PS4)
00540 &+RD*((1-PS1)*(1-PS2)*(1-PS3)*(1-PS4)-R1*R2*R3*R4)
00550 PSS=PSD*(1-P01)*(1-P02)*(1-P03)*(1-P04)+(RD+POD)*PS1*PS2*PS3*PS4
 00560 PPS=PSD*(1-P01*P02*P03*P04)
00570 & +(RD+POD)*(1-(1-PS1)*(1-PS2)*(1-PS3)*(1-PS4)) -PSS
00580 RELECT= PGG**4 + 4*PGG**3*(1-PGG)
00590 & +PGG**2*(4*PPO**2+2*PSS**2+4*PPS*PSS+8*PPO*(PSS+PPS))
00600 & +PGG*PPO*(4*(PSS**2+2*PSS*PPS)+8*PPO*PSS)
```

* * * *

Table A-4. Shunt Regulator Reliability Program (Cont'd)

* * * *

FILE SREL-71 LISTING 12/16/71 11.163 PAGE 03

```
00610 RSHUNT=RBANK(1)*RBANK(2)*RBANK(3)*RBANK(4)*RELECT
00620 IF(TX.GT.10)RSHUNT=RSHUNT
00630 &+RD**4*RQ1*RRES**NRES(1)*(RRES**(NRES(2)+NRES(3))*RQ2*RQ3*
 00640 &(2*P04*P04-P04**4)+RRES**(NRES(2)+NRES(4))*RQ2*(2*P03*P03-
 00650 &P03**4)*RQ4+RRES**(NRES(3)+NRES(4))*(2*P02*P02-P02**4)
00660 &*RQ3*RQ4)
00670 FACTCAP=1 ; RCAP=DEXP(-T*YCAP)
00680 RCAPB=RCAP**NCAP
00690 IF(NFCAP.EQ.0)GO TO 201
00700 DO 202 KK=1,NFCAP
00710 FACTCAP=FACTCAP*(NCAP+1-KK)/KK
00720 202 RCAPB=RCAPB+FACTCAP*RCAP**(NCAP-KK)*(1-RCAP)**KK
00730 201 RSHUNT=RSHUNT*RCAPB
00740 101 PRINT 1002,TX,RSHUNT,RELECT,RCAPB,(RBANK(M),M=1,4)
00750 STOP
00760 1001 FORMAT(1H&,F10.3," : ")
00770 1002 FORMAT(1H0,F5.2,F13.9,/,1H ,6F11.6)
00780 1003 FORMAT(1H ,"                1  2  3  4",/,1H )
00790 END
END OF FILE SREL-71
```

Table A-5. Shunt Regulator Reliability Program Printout -
Using High Failure Rates
Retiability at Time t Before Allowing Failures

```
12/16/71  16.885


LAMBDAS-FAILURES/MILLION HOURS
 ELECTRONICS DATA-LAMBDA,% OPEN-DRIVE,STRINGS-1,2,3,4
 = 0.389, .5,  0.55775,.654, 0.5065,.709, 0.4865,.697, 0.4865,.697

 POWER RESISTOR LAMBDA.%OPEN= .09, .90

 BANK DATA-# PARALLEL STRINGS/BANK-1,2,3,4= 11, 9, 9, 9

 CAPACITOR BANK-LAMBDA,# CAPS,# ALLOWED TO FAIL= 0.018, 4, 1

 TIMES(YEARS)-START,STOP,# PRINTOUTS= 1.14, 11.41, 10

 TIME(YEARS):ALLOWED FAILURES-BANK
                  1  2  3  4
     1.140  : = 1  0  0  1
     2.281  : = 1  1  0  1
     3.422  : = 1  1  1  1
     4.563  : = 1  1  1  1
     5.704  : = 1  1  1  1
     6.846  : = 2  1  1  1
     7.987  : = 2  1  1  2
     9.128  : = 2  2  1  2
    10.269  : = 2  2  2  2
    11.410  : = 2  2  2  2

 TIME   SHUNT REL
         RE       RCAPS        RB1          RB2          RB3          RB4

  1.14  0.969743013
   0.998652   1.000000   0.999857   0.985536   0.985536   0.999906

  2.28  0.964937627
   0.994782   0.999999   0.999436   0.999629   0.971269   0.999529

 3.42  0.984949432
   0.988643   0.999998   0.998744   0.999172   0.999172   0.999172

  4.56  0.974029459
   0.980471   0.999997   0.997792   0.998542   0.998542   0.998542

  5.70  0.960634112
   0.970485   0.999995   0.996588   0.997742   0.997742   0.997742

  6.85  0.949510075
   0.958890   0.999993   0.999856   0.996779   0.996779   0.996779

  7.99  0.937342174
   0.945874   0.999990   0.999775   0.995655   0.995655   0.999882

  9.13  0.925732151
   0.931611   0.999988   0.999669   0.999826   0.994377   0.999826

 10.27  0.918292455
   0.916262   0.999984   0.999535   0.999756   0.999756   0.999756

 11.41  0.902117901
   0.899976   0.999981   0.999370   0.999669   0.999669   0.999669
```

Table A-6. Shunt Regulator Reliability Program Printout - Using High Failure Rates
Reliability at Time t After Allowing Failures

```
12/16/71  16.966


LAMBDAS-FAILURES/MILLION HOURS
 ELECTRONICS DATA-LAMBDA,% OPEN-DRIVE,STRINGS-1,2,3,4
 = 0.389,.5, 0.55775,.654, 0.5065,.709, 0.4965,.697, 0.4865,.697

 POWER RESISTOR LAMBDA,%OPEN= .09, .90
 BANK DATA-# PARALLEL STRINGS/BANK-1,2,3,4= 11, 9, 9, 9

 CAPACITOR BANK-LAMBDA,# CAPS,# ALLOWED TO FAIL= 0.019, 4, 1

 TIMES(YEARS)-START,STOP,# PRINTOUTS= 1.14, 11.41, 10

 TIME(YEARS):ALLOWED FAILURES-BANK
                    1  2  3  4
      1.140  : = 1  0  0  0
      2.281  : = 1  0  0  1
      3.422  : = 1  1  0  1
      4.563  : = 1  1  1  1
      5.704  : = 1  1  1  1
      6.846  : = 1  1  1  1
      7.987  : = 2  1  1  1
      9.128  : = 2  1  1  2
     10.269  : = 2  2  1  2
     11.410  : = 2  2  2  2

 TIME   SHUNT REL
          RE       RCAPS          RB1          RB2          RB3          RB4

  1.14  0.955806129
   0.999652    1.000000    0.999857    0.999536    0.999536    0.999536

  2.28  0.937561646
   0.994782    0.999999    0.999436    0.971269    0.971269    0.999629

  3.42  0.943593354
   0.998643    0.999998    0.998744    0.999172    0.957209    0.999172

  4.56  0.974029459
   0.998471    0.999997    0.997792    0.998542    0.998542    0.998542

  5.70  0.960634112
   0.970485    0.999995    0.996588    0.997742    0.997742    0.997742

  6.85  0.945033617
   0.958890    0.999993    0.995142    0.996779    0.996779    0.996779

  7.99  0.933379836
   0.945874    0.999990    0.999775    0.995655    0.995655    0.995655

  9.13  0.920686722
   0.931611    0.999988    0.999669    0.994377    0.994377    0.999826

 10.27  0.912061006
   0.916262    0.999984    0.999535    0.999756    0.992948    0.999756

 11.41  0.902117901
   0.899976    0.999981    0.999370    0.999669    0.999669    0.999669
```

Table A-7. Shunt Regulator Reliability Program Printout - Using Low Failure Rates
Reliability at Time t Before Allowing Failures

```
12/16/71  10.974


LAMBDAS-FAILURES/MILLION HOURS
 ELECTRONICS DATA-LAMBDA,% OPEN-DRIVE,STRINGS-1,2,3,4
 = 0.126, .5,  0.1135, .756,  0.111, .806,  0.106, .797,  0.106, .797

 POWER RESISTOR LAMBDA.%OPEN= 0.03, .90

 BANK DATA-# PARALLEL STRINGS/BANK-1,2,3,4= 11, 9, 9, 9

 CAPACITOR BANK-LAMBDA,# CAPS,# ALLOWED TO FAIL= 0.008, 4, 1

 TIMES(YEARS)-START,STOP,# PRINTOUTS= 1.14, 11.41, 10

 TIME(YEARS):ALLOWED FAILURES-BANK
                1  2  3  4
    1.140  : = 1  0  0  1
    2.281  : = 1  1  0  1
    3.422  : = 1  1  1  1
    4.563  : = 1  1  1  1
    5.704  : = 1  1  1  1
    6.846  : = 2  1  1  1
    7.987  : = 2  1  1  2
    9.128  : = 2  2  1  2
   10.269  : = 2  2  2  2
   11.410  : = 2  2  2  2

 TIME   SHUNT REL
         RE       RCAPS          RB1          RB2          RB3          RB4

 1.14  0.990239017
   0.999931   1.000000   0.999984   0.995155   0.995155   0.999990

 2.28  0.989911176
   0.999725   1.000000   0.999936   0.999958   0.990329   0.999958

 3.42  0.998962522
   0.999386   1.000000   0.999857   0.999906   0.999906   0.999906

 4.56  0.998166725
   0.998917   0.999999   0.999747   0.999834   0.999834   0.999834

 5.70  0.997153148
   0.998321   0.999999   0.999606   0.999741   0.999741   0.999741

 6.85  0.996483184
   0.997601   0.999999   0.999994   0.999629   0.999629   0.999629

 7.99  0.995740242
   0.996760   0.999998   0.999991   0.999496   0.999496   0.999995

 9.13  0.995117813
   0.995801   0.999998   0.999986   0.999993   0.999344   0.999993

10.27  0.994971730
   0.994727   0.999997   0.999991   0.999993   0.999990   0.999990

11.41  0.993928513
   0.993540   0.999996   0.999974   0.999986   0.999986   0.999986
```

Table A-8. Shunt Regulator Reliability Program Printout - Using Low Failure Rates Reliability at Time t After Allowing Failures

```
12/16/71  11.086


LAMBDAS-FAILURES/MILLION HOURS
 ELECTRONICS DATA-LAMBDA,% OPEN-DRIVE,STRINGS-1,2,3,4
 = 0.126, .5,  0.1135, .756,  0.111, .706,  0.126, .797,  0.105, .797

 POWER RESISTOR LAMBDA.%OPEN= 0.03, .90

 BANK DATA-# PARALLEL STRINGS/BANK-1,2,3,4= 11, 9, 9, 9

 CAPACITOR BANK-LAMBDA,# CAPS,# ALLOWED TO FAIL= 0.009, 4, 1

 TIMES(YEARS)-START,STOP,# PRINTOUTS= 1.14, 11.41, 10

 TIME(YEARS):ALLOWED FAILURES-BANK
                    1  2  3  4
     1.140  : = 1   0  0  0
     2.281  : = 1   0  0  1
     3.422  : = 1   1  0  1
     4.563  : = 1   1  1  1
     5.704  : = 1   1  1  1
     6.846  : = 1   1  1  1
     7.987  : = 2   1  1  1
     9.128  : = 2   1  1  2
    10.269  : = 2   2  1  2
    11.410  : = 2   2  2  2

 TIME   SHUNT REL
          RE        RCAPS          RB1          RB2          RB3          RB4

 1.14  0.985451736
   0.999931    1.000000    0.999984    0.995155    0.995155    0.995155

  2.28  0.980378836
   0.999725    1.000000    0.999936    0.990329    0.990329    0.999953

 3.42  0.984596498
   0.999386    1.000000    0.999857    0.999906    0.995527    0.999906

 4.56  0.988166725
   0.998917    0.999999    0.999747    0.999834    0.999834    0.999834

 5.70  0.997153148
   0.998321    0.999999    0.999606    0.999741    0.999741    0.999741

 6.85  0.995926134
   0.997601    0.999999    0.999435    0.999629    0.999629    0.999629

 7.99  0.995243251
   0.996760    0.999998    0.999991    0.999496    0.999496    0.999496

 9.13  0.994471878
   0.995301    0.999998    0.999986    0.999344    0.999344    0.999993

10.27  0.994158104
   0.994727    0.999997    0.999981    0.999990    0.999172    0.999990

11.41  0.993828513
   0.993540    0.999996    0.999974    0.999996    0.999986    0.999986
```

Table A-9. Markov Chain Analysis

A system can be characterized by a probability state vector [S]. For example a component could be good (S_1), failed open (S_2), or failed short (S_3). The values S_1 - S_3 correspond to the probability of the component being in that state, hence $S_1 + S_2 + S_3 = 1$.

A transition matrix [T] can be assumed, corresponding to a time interval Δt. The transition matrix value is also 1 and corresponds to the time interval probabilities of changing states. For an example the T matrix would be:

$$\begin{bmatrix} T_{1\,1} & T_{1\,2} & T_{1\,3} \\ T_{2\,1} & T_{2\,2} & T_{2\,3} \\ T_{3\,1} & T_{3\,2} & T_{3\,3} \end{bmatrix}$$

where:

$T_{1\,1}$ = Probability of remaining good

$T_{1\,2}$ = Probability of good component failing open

$T_{1\,3}$ = Probability of good component failing short

$T_{2\,1}$ = Probability of open component becoming good

$T_{2\,2}$ = Probability of open component remaining open

$T_{2}\,3$ = Probability of open component becoming short

and so on for $T_{3\,1}$ - $T_{3\,3}$

Typically the T matrix for a component with exclusive short/open failures would be:

$$\begin{bmatrix} e^{-\lambda c \Delta t} & \%\ \text{Open}\ (1-e^{-\lambda c \Delta t}) & \%\ \text{Short}\ (1-e^{-\lambda c \Delta t}) \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The component reliability could then be computed by:

$$[S]_{i+1} = [S]_i \times [T]_{\Delta ti} \qquad i = 0, 1, 2, 3, \ldots, (NT-1)$$

where: NT = Total Mission Time/Δt

The reliability in the example would be S_{1i}, the probability the component is good at any time, T_i, in the mission.

For the simple component example above $[T]_{\Delta ti}$ is the same for all Δt_i, but in a complex system the transition matrix changes with time, hence the general expression $[T]\Delta t_i$.

Table A-10. Current Throttle/Steering Switch Reliability Equations

The following defines the state vectors for the two Current Throttles and the Steering Switch.

At any time t, the probability of RTG power passing through a Current Throttle to the Main Bus is $S_1 + S_2 + S_3 + S_4$. The probability of a good Current Throttle to regulate the Protected Bus during a Main Bus overload is $S_1 + S_3$.

S_1 = Operating on good CT 1

S_2 = Operating on shorted CT 1

S_3 = Operating on good CT 2

S_4 = Operating on shorted CT 2

S_5 = CT path open

These states are calculated at time t by the matrix product expressed below.

$$[S]_t = [S]_{t-\Delta t} \times [T]_{\Delta t}$$

where $[S]_t$ = state matrix at time t

$[S]_{t-\Delta t}$ = state matrix at previous time $t-\Delta t$

$[T]_{\Delta t}$ = transition matrix

The time interval Δt equal to 100 hours was used in the computer calculations.

The transition matrix elements are defined as follows:

Table A-10. Current Throttle/Steering Switch
Reliability Equations (Cont)

T_{11} (Probability remaining on good CT1)

$$T_{11} = RCT_{\Delta t} \cdot PNOWO_{\Delta t} \cdot RSWO_{\Delta t}$$

where: $RCT_{\Delta t}$ = reliability of current throttle for Δt ($e^{-\lambda ct \Delta t}$)

$PNOWO_{\Delta t}$ = probability of no wrong output from failure detector during Δt

$RSWO_{\Delta t}$ = probability of switch not failing open during Δt

T_{12} (prob of going to shorted CT 1 operation)

$$T_{12} = PSCT_{\Delta t} \cdot PNO_t \cdot RSWO_{\Delta t}$$

where:

$PSCT_{\Delta t}$ = Probability CT 1 shorts during Δt

PNO_t = Probability failure detector has failed (no output) by time t

T_{13} (prob. of going to CT 2 operation)

$$T_{13} = [PWO_{\Delta t} + (PFO_{\Delta t} + QCT_{\Delta t}) \cdot RFD] \cdot RSWOVER_t \cdot RDCT_t$$

where:

$PWO_{\Delta t}$ = Probability of wrong failure detector output during Δt

$PFO_{\Delta t}$ = Probability of switch failure open during Δt

$QCT_{\Delta t}$ = Probability of CT 1 failure during Δt

RFD_t = Reliability of failure detector at time t

$RSWOVER_t$ = Probability relay will transfer at time t

B-2

Table A-10. Current Throttle/Steering Switch Reliability Equations (Cont)

$RDCT_t$ = Reliability of dormant CT 2 at time t = $e^{\frac{-\lambda ct}{10}}$ t

T_{14} (Probability of going to shorted CT 2 operation from good CT 1)

$T_{14} = (PWO_{\Delta t} + (PFO_{\Delta t} + QCT_{\Delta t}) \cdot RFD_t) \cdot PSWOVER_t \cdot QSDCT_t$

where:

$QSDCT_t$ = Probability dormant CT 2 has failed short = (1-% open) (1-RDCT)

T_{15} (Probability of failure while operating on CT 1)

$T_{15} = 1 - T_{11} - T_{12} - T_{13} - T_{14}$

$T_{21} = \emptyset$

T_{22} (Prob. remaining on shorted CT 1)

$T_{22} = RSWO_{\Delta t}$

T_{23} = (Prob. going to CT 2 from shorted CT 1)

$T_{23} = \emptyset$

$T_{24} = \emptyset$

$T_{25} = 1-T_{22}$

$T_{31} = \emptyset$, $T_{32} = \emptyset$

T_{33} (Prob. remaining on good CT 2)

$T_{33} = RCT_{\Delta t} \cdot RSWO_{\Delta t}$

$T_{34} = QSCT_{\Delta t} \cdot RSWO_{\Delta t}$

$T_{35} = 1 - T_{33} - T_{34}$

$T_{41} = T_{42} = T_{43} = \emptyset$

$T_{44} = RSWO_{\Delta t}$

$T_{51} = T_{52} = T_{53} = T_{54} = \emptyset$

T_{55} (Prob. remaining failed) = 1

Table A-11. Inverter Function Calculations

The inverters, switches, command generators, and failure detection circuitry were defined by 4 modes - operating on inverter 1, operating on 2, operating on 3, not operating (failed). Thus the function was described by the state vector: $[S_1\ S_2\ S_3\ S_4]$.

The transition matrix was calculated using all the above expressions. The T matrix components were:

T_{11} - Probability of remaining of inverter 1

T_{12} - Probability of switching from inverter 1 to inverter 2

T_{13} - Probability of switching from inverter 1 to inverter 3

T_{14} - Probability of function failure while operating on inverter 1

T_{21} - $\emptyset$

T_{22} - Probability of staying on inverter 2

T_{23} - Probability of switching from 2 to 3

T_{24} - Probability of function failure while operating on inverter 2

T_{31} - $\emptyset$

T_{32} - $\emptyset$

Due to failure detection and switching arrangement no returns to previously used inverter are possible

T_{33} - Probability of remaining on inverter 3

T_{34} - Probability of function failure while operating on inverter 3

T_{41} - $\emptyset$

T_{42} - $\emptyset$

T_{43} - $\emptyset$

T_{44} - 1 - Probability of remaining failed

Table A-11. Inverter Function Calculations (Cont)

The elements were calculated by:

$$T_{11} = RINV_{\Delta t} \cdot PNOWO_{\Delta t} \cdot RF12_{\Delta t} \cdot PNOS3_{\Delta t}$$

where:

$RINV_{\Delta t}$ = Reliability of operating inverter for time Δt ($e^{-\lambda inv \Delta t}$)

$PNOWO_{\Delta t}$ = Probability of no wrong output from majority vote failure detector during Δt

$RF12_{\Delta t}$ = Probability no failure causing switchover occurs in inverter 1, 2 switches/command generator during Δt

$PNOS3_{\Delta t}$ = Probability the input switch to inverter 3 does not fail closed during Δt

$$T_{12} = (QINV_{\Delta t} + PF12_{\Delta t} - QINV_{\Delta t} \cdot PF12_{\Delta t}) \cdot RMV_t \cdot PSWOVER_t \cdot RDCG_t \cdot PNOS3_{\Delta t} \cdot RDINV_t$$

where:

$QINV_{\Delta t}$ - Probability inverter 1 fails during Δt

$PF12_{\Delta t}$ - Probability a failure causing switchover occurs in inverter 1, 2 switches and command generator during Δt

RMV_t - Probability that the majority vote failure detector works at time t

$PSWOVER_t$ - Probability successful turn-on of inverter 2 and turn-off of inverter 1 if commanded at time t

$RDCG_t$ - Probability of no erroneous output (s) from dormant command generator which has just been turned on at time t

RDINV - Reliability of previously dormant inverter at time t ($e^{-\frac{\lambda inv}{10} t}$)

Table A-11. Inverter Function Calculations (Cont)

$$T_{13} = \overbrace{(QINV_{\Delta t} \cdot QDINV_t \cdot RMV_t}^{\text{Turn on bad Inverter 2}} + \overbrace{PWO_{\Delta t} \cdot RINV_{\Delta t}}^{\text{Failure Detector Failure}}$$

$$+ \overbrace{QINV_{\Delta t} \cdot RMV_t \cdot PSCG_t}^{\text{Command Generator Failure}} \cdot PSWOVER_t \cdot P2SWOVER_t \cdot RDINV_t$$

where:

$PWO_{\Delta t}$ - Probability of failed short failure detector during Δt

$PSCG_t$ - Probability previously dormant command generator provides erroneous output when turned on at time t

$P2SWOVER_t$ - Probability second command generator and inverter 2, 3 switches successfully turn inverter 2 off and inverter 3 on at time t

$$T_{14} = 1 - T_{11} - T_{12} - T_{13}$$

$$T_{21} = \emptyset$$

$$T_{22} = RINV_{\Delta t} \cdot PNOWO_{\Delta t} \cdot PNOS1_{\Delta t} \cdot RF23_{\Delta t}$$

$$T_{23} = (QINV_{\Delta t} + PF23_{\Delta t} \cdot RMV_t + PWO_{\Delta t}) \cdot P2SWOVER_t \cdot RDINV$$

$$T_{24} = 1 - T_{22} - T_{23}$$

$$T_{31} = T_{32} = \emptyset$$

$$T_{33} = RINV_{\Delta t} \cdot PNOS1_{\Delta t} \cdot PNOS2_{\Delta t} \cdot PNOF3_{\Delta t}$$

where:

$PNOF3_{\Delta t}$ = Probability of no failure open in inverter 3 switch function during Δt

A-11. Inverter Function Calculations (Cont)

$T_{34} = 1 - T_{33}$

$T_{41} = T_{42} = T_{43} = \emptyset$

$T_{44} = 1$

The same program was used to analyze two inverter case by setting key variables to 1 or $\emptyset$. The reliability of the third inverter switches and second command generator were set to 1 and the failure detector failures added to the probability of going to inverter 2.

Table A-12. Inverter Reliability Program

* * * *

FILE TOPS-REL LISTING 12/22/71 PAGE 01

```
00001 *****  TJE 20 DEC 1971
00010 COMMON SMA,SMB,SMC,UTMA,UTMB,UTMC,RCG,QOCG,QSCG,SCG,PSCG,
00020 &SSTT,ASK,A,AA,RINV,QINV,RDINV,RMV,RDTPWO,PSWOVER,P2SWOVER,
00030 &P23OVER,RFDELT,RCFDELT
00040 DOUBLE PRECISION RRELAY,QP,QK,RD,QOD,QSD,S(4,4),CTM(4,4),OTM(4,4),
 00050 &SMA(4,3),UTMA(4,3),SMB(4,3),UTMB(4,3),SMC(4,3),UTMC(4,3),PM(3,3)
 00060 &PI2,PI3,P23,RINV,QINV,RDINV,QDINV,RMV,PWO,PNO,DTPWO,RCG,QOCG,
00070 &QSCG,SSTT(4,4),SSSM(4),PKO,POMSW,PSSBYSW,RFD,QOFD,QSFD,PSSBY2SW,
 00080 &PF1,PF2,P1WORK,PSWOVER,RSBY2SW,PSSWC,P2WORK,P2SWOVER
00090 &,PCF2,PCF1,RCFDELT,P23WORK,PKCG,POSBYSW,PSC2,PCTRNON,P23OVER,
00100 &SCG(2,3),PSCG(3),DTRCG,DTQOCG,DTQSCG,NSSSM(4),R3SBY2SW,R3MSW,
00110 &R3SBYSW,R3A1,R3A2,R3B1,R3B2,R3C1,R3C2,PKO2,YOD,YOFD,YOCG,
00120 &QSFD,QC,PTRNON,RFDELT,RINVFUNC,X2INV,R2A1,R2A1,R2MSW
00130 &,PWO1,RDTPWO,PKS
00140 ASCII A(6),AA(4),ASK(6)
00150    PRINT:" TOPS MAIN BUS INVERTER FUNCTION RELIABILITY"
00160    PRINT:" " ; PRINT:"DO YOU WANT RELAY STATUS,DIAGNOSTIC PRINT
 00170 & OUTS(TWO ANSWERS)?" ; READ:ASK(1),ASK(2)
00180 IF(ASK(1).EQ."YES")IDPR=1 ; IF(ASK(2).EQ."YES")IDPR=1
00190    PRINT:"# INVERTERS(2 OR 3)" ; READ:NINV ; IF(NINV.LT.2)STOP
00200    PRINT:"QUAD COMMAND GENERATOR?(YES OR NO)" ; READ:ASK(3)
00210    A(1)="SMA" ; A(2)="SMB" ; A(3)="SMC"
00220    A(4)="UTMA" ; A(5)="UTMB" ; A(6)="UTMC"
00230    AA(1)="S1-" ; AA(2)="S2-" ; AA(3)="S3-" ; AA(4)="FAIL"
00240    PRINT:" LAMBDAS IN FAILURES PER MILLION HOURS"
00250    PRINT:"LAMBDAS-RELAY,INVERTER" ; READ:YR,YINV
00260    PRINT:"LAMBDAS,P OPEN-RELAY DRIVER,FAILURE DETECTOR,
00270 &COMMAND GENERATOR"  ;  PRINT:" "
00280    READ:YD,YOD,YFD,YOFD,YCG,YOCG
00290    YR=YR/1000000 ; YD=YD/1000000
```

* * * *

Table A-12. Inverter Reliability Program (Cont)

* * * *

FILE TOPS-REL LISTING PAGE 02

```
00300     YINV=YINV/1E6  ;  YFD=YFD/1E6  ;  YCG=YCG/1E6
00310 PRINT:" MISSION HOURS, # INTERVALS"  ;  READ:TEND,NIT
00320 DT=TEND/NIT  ;  T=0
00330     KK=0
00340     RINV=DEXP(-DT*YINV)  ;  QINV=1-RINV
00350     X2INV=1
00360     DTRCG=DEXP(-DT*YCG) ; DTQOCG=YOCG*(1-DTRCG)
00370     DTQSCG=1-DTRCG-DTQOCG
00380     PF1=0;PWO1=0;PSSWC=0;PCF1=0
00390     P12=1E-12 ;R3A1=1;R2A1=1;R3C2=1;R3B2=1
00400     P13=P12  ;  P23=P12
00410 DO 9 M=1,4 ; DO 9 N=1,3 ; SMA(M,N)=0 ; SMB(M,N)=0
00420     SMC(M,N)=0  ;  9 SSSM(M)=0
00430     SMA(1,1)=1;SMB(1,1)=1;SMC(1,1)=1;SSSM(1)=1
00440     DO 10 I=1,NIT
00450 DO 22 IS=1,4
00460 S(IS,1)=S(IS,3)  ;  22 S(IS,2)=S(IS,4)
00470     KK=KK+1  ;  K=3
00480     T=T+DT ; TY=T/(24*365.25)
00490     RRELAY=DEXP(-T*YR) ; QR=1-RRELAY
00500     RD=DEXP(-T*YD) ; QOD=YOD*(1-RD) ; QSD=1-RD-QOD
00510     QC=.05*QR
00520     QK=.9*QR
00530 ** OPEN RELAY **
00540     S(1,K)=RRELAY*RD*RD
00550     S(3,K)=(QC+QOD-QC*QOD+(1-QC)*QSD*(1-.5*(1-QC)*QSD))*(1-QK)
00560 &          +0.9*QK
00570     S(4,K)=(1-QC)*QSD*(1-.5*(1-QC)*QSD)*(1-QK)
00580     S(2,K)=1-S(1,K)-S(3,K)-S(4,K)
00590     K=K+1
```

* * * *

Table A-12. Inverter Reliability Program (Cont)

* * * *

FILE TOPS-REL LISTING PAGE 03

```
00600 ** CLOSED RELAY **
00610     S(1,K)=RRELAY*RD*RD
00620     S(3,K)=(1-QC)*QSD*(1-.5*(1-QC)*QSD)*(1-QK)+0.4*QK
00630     S(4,K)=(QC+QO-QC*QOD+(1-QC)*QSD*(1-.5*(1-QC)*QSD))*(1-QK)
00640     S(2,K)=1-S(1,K)-S(3,K)-S(4,K)
00650 IF(I.EQ.1)GO TO 10
00660     OTM(1,1)=S(1,3)/S(1,1)  ;  CTM(1,1)=S(1,4)/S(1,2)
00670     OTM(1,3)=(S(3,3)-S(3,1))/(S(1,1)+S(2,1))
00680     OTM(1,4)=(S(4,3)-S(4,1))/(S(1,1)+S(2,1))
00690     OTM(1,2)=1-OTM(1,1)-OTM(1,3)-OTM(1,4)
00700     OTM(2,3)=OTM(1,3)  ;  OTM(2,4)=OTM(1,4)
00710     OTM(2,2)=1-OTM(2,3)-OTM(2,4)
00720     OTM(3,3)=1  ;  OTM(4,4)=1
00730     CTM(1,3)=(S(3,4)-S(3,2))/(S(1,2)+S(2,2))
00740     CTM(1,4)=(S(4,4)-S(4,2))/(S(1,2)+S(2,2))
00750     CTM(1,2)=1-CTM(1,1)-CTM(1,3)-CTM(1,4)
00760     CTM(2,3)=CTM(1,3)  ;  CTM(2,4)=CTM(1,4)
00770     CTM(2,2)=1-CTM(2,3)-CTM(2,4)
00780     CTM(3,3)=1 ; CTM(4,4)=1
00790 DO 20 KT=1,4  ;  DO 20 K123=1,3
00800 UTMA(KT,K123)=SMA(KT,K123)  ;  UTMB(KT,K123)=SMB(KT,K123)
00810 UTMC(KT,K123)=SMC(KT,K123)
00820 SMA(KT,K123)=0 ; SMB(KT,K123)=0
00830 20 SMC(KT,K123)=0
00840 DO 21 KT=1,4  ;  DO 21 KKT=1,4
00850 SMA(KT,1)=SMA(KT,1)+UTMA(KKT,1)*CTM(KKT,KT)
00860 SMB(KT,1)=SMB(KT,1)+UTMB(KKT,1)*OTM(KKT,KT)
00870 SMC(KT,1)=SMC(KT,1)+UTMC(KKT,1)*OTM(KKT,KT)
00880 SMA(KT,2)=SMA(KT,2)+UTMA(KKT,2)*OTM(KKT,KT)
00890 SMB(KT,2)=SMB(KT,2)+UTMB(KKT,2)*CTM(KKT,KT)
```

* * * *

Table A-12. Inverter Reliability Program (Cont)

* * * *


```
00900 SMC(KT,2)=SMC(KT,2)+UTMC(KKT,2)*OTM(KKT,KT)
00910 SMA(KT,3)=SMA(KT,3)+UTMA(KKT,3)*OTM(KKT,KT)
00920 SMB(KT,3)=SMB(KT,3)+UTMB(KKT,3)*OTM(KKT,KT)
00930 SMC(KT,3)=SMC(KT,3)+UTMC(KKT,3)*CTM(KKT,KT)
00940 21 CONTINUE
00950    SMA(1,2)=SMA(1,2)+SMA(1,1)*P12
00960    SMB(1,2)=SMB(1,2)+SMB(1,1)*P12
00970    SMC(1,2)=SMC(1,2)+SMC(1,1)*P12
00980    SMA(3,2)=SMA(3,2)+(SMA(2,1)+SMA(3,1))*P12
00990    SMA(4,2)=SMA(4,2)+SMA(4,1)*P12
01000    SMB(3,2)=SMB(3,2)+SMB(3,1)*P12
01010    SMB(4,2)=SMB(4,2)+(SMB(2,1)+SMB(4,1))*P12
01020    SMC(2,2)=SMC(2,2)+SMC(2,1)*P12
01030    SMC(3,2)=SMC(3,2)+SMC(3,1)*P12
01040    SMC(4,2)=SMC(4,2)+SMC(4,1)*P12
01050    SMA(1,3)=SMA(1,3)+SMA(1,2)*P23+SMA(1,1)*P13
01060    SMA(2,3)=SMA(2,3)+SMA(2,2)*P23
01070    SMA(3,3)=SMA(3,3)+SMA(3,2)*P23+(SMA(2,1)+SMA(3,1))*P13
01080    SMA(4,3)=SMA(4,3)+SMA(4,2)*P23+SMA(4,1)*P13
01090    SMB(1,3)=SMB(1,3)+SMB(1,2)*P23+SMB(1,1)*P13
01100    SMB(3,3)=SMB(3,3)+(SMB(3,2)+SMB(2,2))*P23+SMB(3,1)*P13
01110    SMB(4,3)=SMB(4,3)+SMB(4,2)*P23+(SMB(2,1)+SMB(4,1))*P13
01120    SMC(1,3)=SMC(1,3)+SMC(1,2)*P23+SMC(1,1)*P13
01130    SMC(3,3)=SMC(3,3)+SMC(3,2)*P23+SMC(3,1)*P13
01140    SMC(4,3)=SMC(4,3)+(SMC(4,2)+SMC(2,2))*P23
01150 &             +(SMC(4,1)+SMC(2,1))*P13
01160 DO 23 KT=1,4
01170    SMA(KT,1)=SMA(KT,1)*(1-P12-P13)
01180    SMB(KT,1)=SMB(KT,1)*(1-P12-P13)
01190    SMC(KT,1)=SMC(KT,1)*(1-P12-P13)
```

* * * *

Table A-12. Inverter Reliability Program (Cont)

* * * *

FILE TOPS-REL LISTING PAGE 05

```
01200     SMA(KT,2)=SMA(KT,2)*(1-P23)
01210     SMB(KT,2)=SMB(KT,2)*(1-P23)
01220 23  SMC(KT,2)=SMC(KT,2)*(1-P23)
01230  DO 24 N=1,3
01240     PM(1,N)=1/(SMA(1,N)+SMA(2,N)+SMA(3,N)+SMA(4,N))
01250     PM(2,N)=1/(SMB(1,N)+SMB(2,N)+SMB(3,N)+SMB(4,N))
01260 24  PM(3,N)=1/(SMC(1,N)+SMC(2,N)+SMC(3,N)+SMC(4,N))
01270     DO 25 N=1,3
01280     IF(NINV.EQ.2)PM(3,N)=0
01290     DO 25 M=1,4
01300     UTMA(M,N)=PM(1,N)*SMA(M,N)
01310     UTMB(M,N)=PM(2,N)*SMB(M,N)
01320 25  UTMC(M,N)=PM(3,N)*SMC(M,N)
01330     DO 27 N=1,3
01340     27 IF(NINV.EQ.2) UTMC(1,N)=1
01350 **** COMMAND GENERATOR
01360     RCG=DEXP(-T*YCG) ; QOCG=YOCG*(1-RCG) ; QSCG=1-RCG-QOCG
01370     SCG(1,1)=DEXP(-T*YCG/10)
01380     IF(NINV.EQ.2)SCG(1,1)=1
01390     SCG(1,2)=YOCG*(1-SCG(1,1))  ;  SCG(1,3)=1-SCG(1,1)-SCG(1,2)
01400     RDCG=(SCG(1,1)+SCG(1,2))**4
01410     IF(ASK(3).EQ."YES")RDCG=1-(2*SCG(1,2)**2-SCG(1,2)**4)
01420     QSDCG=4*SCG(1,3)
01430 IF(ASK(3).EQ."YES")QSDCG=4*(SCG(1,3)**2-SCG(1,3)**3)+SCG(1,3)**4
 01440     SCG(2,2)=SCG(2,2)+SCG(2,1)*DTQOCG+SCG(1,2)*P12
01450     SCG(2,3)=SCG(2,3)+SCG(2,1)*DTQSCG+SCG(1,3)*P12
01460     SCG(2,1)=SCG(2,1)*DTRCG+SCG(1,1)*P12
01470     PKCG=1/(SCG(2,1)+SCG(2,2)+SCG(2,3))
01480     IF(NINV.EQ.2)PKCG=0
01490     DO 33 ICG=1,3
```

* * * *

Table A-12. Inverter Reliability Program (Cont)

* * * *

FILE TOPS-REL LISTING PAGE 06

```
01500 33 PSCG(ICG)=SCG(2,ICG)*PKCG
01510    IF(NINV.EQ.2)PSCG(1)=1
01520 ***PF
01530    IF(ASK(3).EQ."YES")GO TO 41
01540    P2WORK=UTMB(1,1)**2*UTMC(1,1)**2*(SCG(1,1)+SCG(1,3))
01550    P2SWOVER=P2WORK**4+4*P2WORK**3*(1-P2WORK)
01560    PKO=UTMA(3,1)*(RCG+QOCG)+(1-UTMA(4,1))*QSCG
01570    POMSW=2*(2*PKO**2-PKO**4)-(2*PKO**2-PKO**4)**2
01580    PSSBYSW=UTMB(4,1)*(RCG+QOCG)+(1-UTMB(3,1))*QSCG
01590    PTRNON=4*(PSSBYSW**2-PSSBYSW**3)+PSSBYSW**4
01600    PF2=POMSW+PTRNON-PTRNON*POMSW
01610    RFDELT=(1-PF2)/(1-PF1)  ;  PF1=PF2
01620    P1WORK=(1-UTMA(4,1))**2*(1-UTMB(3,1))**2*(RCG+QSCG)
01630    PSWOVER=P1WORK**4+4*P1WORK**3*(1-P1WORK)
01640    GO TO 42
01650    41 PKO=2*UTMA(3,1)**2-UTMA(3,1)**4
01660    PSSBYSW=4*(UTMB(4,1)**2-UTMB(4,1)**3)+UTMB(4,1)**4
01670    PF2=4*(QSCG**2-QSCG**3)+QSCG**4+2*PKO+PSSBYSW-2*PKO*PSSBYSW
01680    RFDELT=(1-PF2)/(1-PF1)  ;  PF1=PF2
01690    PKS=4*(UTMA(4,1)**2-UTMA(4,1)**3)+UTMA(4,1)**4
01700    PKO=2*UTMB(3,1)**2-UTMB(3,1)**4
01710    PSWOVER=(1-(2*QOCG**2-QOCG**4+4*(QSCG**2-QSCG**3)+QSCG**4))
01720 &          *(1-PKS)**2*(1-PKO)**2
01730    PKO=2*UTMC(3,1)**2-UTMC(3,1)**4
01740 PKS=4*((UTMB(2,1)+UTMB(4,1))**2-(UTMB(2,1)+UTMB(4,1))**3)
01750 &    +(UTMB(2,1)+UTMB(4,1))**4
01760    P2SWOVER=(1-2*SCG(1,2)**2+SCG(1,2)**4)*(1-PKO)**2*(1-PKS)**2
 01770 42 RDINV=DEXP(-T*YINV/10)
01780    RFD=DEXP(-T*YFD) ; QOFD=YOFD*(1-RFD) ; QSFD=1-RFD-QOFD
01790    PNO=3*QOFD**2-QOFD**3 ; PWO=3*QSFD**2-QSFD**3
```

* * * *

C

Table A-12. Inverter Reliability Program (Cont)

* * * *


```
01800     RDTPWO=(1-PWO)/(1-PWO1)  ;  PWO1=PWO
01810     IF(NINV.EQ.2)X2INV=RDTPWO
01820     RMV=1-PNO-PWO
01830     IF(NINV.EQ.2)P2SWOVER=0
01840     PSSBY2SW=4*(UTMC(4,1)**2-UTMC(4,1)**3)+UTMC(4,1)**4
01850     RSBY2SW=(1-PSSBY2SW)/(1-PSSWC)  ;  PSSWC=PSSBY2SW
01860 *** FIRST LINE T MATRIX
01870     SSTT(1,1)=RINV*RDTPWO*RFDELT*RSBY2SW
01880     SSTT(1,2)=(QINV+(1-RFDELT)-QINV*(1-RFDELT))*RMV*PSWOVER
01890 &     *RDCG*RSBY2SW*RDINV
01900     IF(NINV.EQ.2)SSTT(1,2)=SSTT(1,2)+(1-RDTPWO)*PSWOVER*RDINV
01910     P12=SSTT(1,2)
01920     SSTT(1,3)=((1-RDTPWO)*RINV+QINV*(1-RDINV)*RMV+QINV*RMV*QSDCG)*
01930 &       PSWOVER*P2SWOVER*RDINV
01940     P13=SSTT(1,3)
01950     SSTT(1,4)=1-SSTT(1,1)-SSTT(1,2)-SSTT(1,3)
01960 **** 2ND LINE T MATRIX
01970     IF(ASK(3).EQ."YES")GO TO 43
01980     PK02=UTMB(3,2)*(PSCG(1)+PSCG(2))+(1-UTMB(4,2))*PSCG(3)
01990     POSBYSW=2*(2*PK02**2-PK02**4)-(2*PK02**2-PK02**4)**2
02000     PSC2=UTMC(4,2)*(PSCG(1)+PSCG(2))+(1-UTMC(3,2))*PSCG(3)
02010     PCTRNON=4*(PSC2**2-PSC2**3)+PSC2**4
02020     PCF2=POSBYSW+PCTRNON-PCTRNON*POSBYSW
02030     RCFDELT=(1-PCF2)/(1-PCF1)  ;  PCF1=PCF2
02040     P23WORK=(1-UTMB(4,2))**2*(1-UTMC(3,2))**2*(PSCG(1)+PSCG(3))
02050     P23OVER=P23WORK**4+4*P23WORK**3*(1-P23WORK)
02060     GO TO 44
02070 43  PK02=2*UTMB(3,2)**2-UTMB(3,2)**4
02080     PSC2=4*(UTMC(4,2)**2-UTMC(4,2)**3)+UTMC(4,2)**4
02090     PCF2=4*(PSCG(3)**2-PSCG(3)**3)+PSCG(3)**4+
```

* * * *

Table A-12. Inverter Reliability Program (Cont)

* * * *


```
02100 &       2*PKO2+PSC2-2*PKO2*PSC2
02110     RCFDELT=(1-PCF2)/(1-PCF1)  ;  PCF1=PCF2
02120     PKS=4*(UTMB(4,2)**2-UTMB(4,2)**3)+UTMB(4,2)**4
02130     PKO=2*UTMC(3,2)**2-UTMC(3,2)**4
02140 P23OVER=(1-2*PSCG(2)**2+PSCG(2)**4)*(1-PKS)**2*(1-PKO)**2
02150 44 IF(NINV.EQ.2)P23OVER=0
02160 ***MAIN SWITCHES
02170     R2A2=1-(4*(UTMA(4,2)**2-UTMA(4,2)**3)+UTMA(4,2)**4)
02180     R2MSW=R2A2/R2A1  ;  R2A1=R2A2
02190     R3A2=1-(4*(UTMA(4,3)**2-UTMA(4,3)**3)+UTMA(4,3)**4)
02200     R3MSW=R3A2/R3A1  ;  R3A1=R3A2
02210     SSTT(2,2)=RINV*RDTPWO*R2MSW*RCFDELT/X2INV
02220     SSTT(2,3)=(QINV+(1-RCFDELT)*RMV+(1-RDTPWO))*P23OVER*RDINV
02230     P23=SSTT(2,3)
02240     SSTT(2,4)=1-SSTT(2,2)-SSTT(2,3)
02250 *** THIRD LINE T MATRIX
02260     R3C1=1-(2*UTMC(3,3)**2-UTMC(3,3)**4)
02270     R3SBY2SW=R3C1/R3C2  ;  R3C2=R3C1
02280     R3B1=1-(4*(UTMB(4,3)**2-UTMB(4,3)**3)+UTMB(4,3)**4)
02290     R3SBYSW=R3B1/R3B2  ;  R3B2=R3B1
02300     SSTT(3,3)=RINV*(R3SBY2SW*R3MSW*R3SBYSW)**2
02310     SSTT(3,4)=1-SSTT(3,3)
02320     SSTT(4,4)=1
02330     DO 31 KSS=1,4  ;  NSSSM(KSS)=SSSM(KSS)
02340 31 SSSM(KSS)=0
02350     DO 32 KSS=1,4  ;  DO 32 KKSS=1,4
02360 32 SSSM(KSS)=SSSM(KSS)+NSSSM(KKSS)*SSTT(KKSS,KSS)
02370     RINVFUNC=1-SSSM(4)
02380     IF(KK.LT.NIT/10)GO TO 10  ;  KK=0
02390     PRINT 100,TY,RINVFUNC
```

* * * *

Table A-12. Inverter Reliability Program (Cont)

* * * *

FILE TOPS-REL LISTING PAGE 09

```
02400 PRINT:"STATE MATRIX-1,2,3,FAILED"
02410 PRINT 104,(SSSM(M),M=1,4)
02420 IF(I.EQ.NIT)ASK(1)="YES" ; IF(I.EQ.NIT)ASK(2)="YES"
02430    IF(I.EQ.NIT)IDPR=1
02440    IF(IDPR.EQ.1)CALL PRINTOUT
02450 10 CONTINUE
02460 100 FORMAT(1H0,F8.3,"-YEARS,INV FUNCT. RELIABILITY=",F11.9)
 02470 104 FORMAT(1H ,4F14.9)
02480 END
END OF FILE TOPS-REL
```

Table A-13. Inverter Reliability Program - Subroutine

* * * *

FILE PRINTOUT LISTING 12/22/71 PAGE 01

```
00001 ****** TJE   20 DEC 1971
00010 SUBROUTINE PRINTOUT
00020 COMMON SMA(4,3),SMB(4,3),SMC(4,3),UTMA(4,3),UTMB(4,3),UTMC(4,3),
 00030 &RCG,QOCG,QSCG,SCG(2,3),PSCG(3),SSTT(4,4),ASK(6),A(6),AA(4)
 00040 &,RINV,QINV,RDINV,RMV,RDTPWO,PSWOVER,P2SWOVER,P23OVER,
00050 &RFDELT,RCFDELT
00060 DOUBLE PRECISION SMA,SMB,SMC,UTMA,UTMB,UTMC,RCG,QOCG,QSCG,
00070 &SCG,PSCG,SSTT,RINV,QINV,RDINV,RMV,RDTPWO,PSWOVER,P2SWOVER,
00080 &P23OVER,RFDELT,RCFDELT
00090 ASCII ASK,A,AA
00100 IF(ASK(2).NE."YES")GO TO 10
00110 PRINT:" "
00120 PRINT:"  SUBSYSTEM TRANSITION MATRIX"
00130 PRINT 100,((SSTT(N,M),M=1,4),N=1,4)
00140 PRINT:" " ; PRINT:" FACTORS"
00150 PRINT 101,RINV,QINV,RDINV,RMV,RDTPWO,PSWOVER,P2SWOVER,P23OVER
00160 &,RFDELT,RCFDELT
00170 10 IF(ASK(1).NE."YES")GO TO 11
00180 PRINT:"   COMMAND GENERATOR-G,O,S"
00190 PRINT 100,RCG,QOCG,QSCG
00200 PRINT 100,(SCG(1,M),M=1,3)
00210 PRINT 100,(PSCG(M),M=1,3)
00220 PRINT:"    STATE MATRICES"
00230 PRINT:"   SMA"
00240 PRINT 100,((SMA(M,N),M=1,4),N=1,3)
00250 PRINT:"   SMB"
00260 PRINT 100,((SMB(M,N),M=1,4),N=1,3)
00270 PRINT:"   SMC"
00280 PRINT 100,((SMC(M,N),M=1,4),N=1,3)
00290 PRINT:" " ; PRINT:"   PROBABILITY MATRICES"
```

* * * *

Table A-13. Inverter Reliability Program - Subroutine (Cont)

```
                              *  *  *  *
                        FILE PRINTOUT LISTING                    PAGE 02

00300 PRINT:"      UTMA"
00310 PRINT 100,((UTMA(M,N),M=1,4),N=1,3)
00320 PRINT:"      UTMB"
00330 PRINT 100,((UTMB(M,N),M=1,4),N=1,3)
00340 PRINT:"      UTMC"
00350 PRINT 100,((UTMC(M,N),M=1,4),N=1,3)
00360 11 RETURN
00370 100 FORMAT(1H ,4F13.9)
00380 101 FORMAT(1H ,5F13.9)
00390 END
END OF FILE PRINTOUT
```

Table A-14. Power Subsystem Reliability Program

* * * *

FILE TSS-REL LISTING PAGE 01

```
00010 ***TJE 22 DEC 71
00020 DIMENSION RSHUNT(10),RMINV(10),RPINV(10)
00030 DOUBLE PRECISION RRELAY,QR,QC,RD,QOD,QSD,QK,S(4,4),OTM(4,4),
00040 &CTM(4,4),UTMA(4,2),SMA(4,2),RDIOD,PODIOD,RPD,RCT,RDCT,POCT,
00050 &PSCT,PSDCT,PM(2),SSTT(5,5),SSSM(5),RDTFO,RDTFO2,RDTPWO,NSSSM(5)
00060 &,PFO1,PFO2,PWO,PWO1,PF2O1,PF2O2,P12
00070 ASCII ASK
00080 PRINT:"  TOPS POWER SUBSYSTEM RELIABILITY"
00090 PRINT:" " ; PRINT:" LONG FORM PRINTOUT?(YES OR NO)"
00100 READ:ASK
00110 PRINT:" LAMBDAS-RTG,RELAY" ; READ:YRTG,YR
00120 PRINT:"LAMBDAS,P OPEN-C.T.,ST.SW.,RELAY DRVR,POW DIODES"
00130 PRINT:" " ; READ:YCT,YOCT,YSTSW,YOSTSW,YD,YOD,YDIOD,YODIOD
00140 YR=YR/1000000  ;  YD=YD/1000000
00150 PRINT:"   RELIABILITIES"
00160 PRINT:" SHUNT" ; READ:(RSHUNT(M),M=1,10)
00170 PRINT:" MAIN INV FUNC" ; READ:(RMINV(M),M=1,10)
00180 PRINT:" PB INV FUNC" ; READ:(RPINV(M),M=1,10)
00190 DT=100 ; T=0  ;  NIT=1000
00200 RCT=DEXP(-DT*YCT/1000000)
00210 POCT=YOCT*(1-RCT) ; PSCT=1-RCT-POCT
00220 SMA(1,1)=1  ;  SSSM(1)=1  ;  SSTT(5,5)=1
00230 P12=1E-12
00240 DO 10 IX=1,NIT
00250 KK=KK+1
00260 T=T+DT
00270 **CURRENT THROTTLE
00280 DO 22 IS=1,4
00290 S(IS,1)=S(IS,3) ;  22 S(IS,2)=S(IS,4)
00300    RRELAY=DEXP(-T*YR) ; QR=1-RRELAY
```

* * * *

Table A-14. Power Subsystem Reliability Program (Cont)

* * * *


```
00310     RD=DEXP(-T*YD) ; QOD=YOD*(1-RD) ; QSD=1-RD-QOD
00320     QC=.05*QR
00330     QK=.9*QR
00340 K=3
00350 ** OPEN RELAY **
00360     S(1,K)=RRELAY*RD*RD
00370     S(3,K)=(QC+QOD-QC*QOD+(1-QC)*QSD*(1-.5*(1-QC)*QSD))*(1-QK)
00380 &          +0.9*QK
00390     S(4,K)=(1-QC)*QSD*(1-.5*(1-QC)*QSD)*(1-QK)
00400     S(2,K)=1-S(1,K)-S(3,K)-S(4,K)
00410     K=K+1
00420 ** CLOSED RELAY **
00430     S(1,K)=RRELAY*RD*RD
00440     S(3,K)=(1-QC)*QSD*(1-.5*(1-QC)*QSD)*(1-QK)+0.4*QK
00450     S(4,K)=(QC+QO-QC*QOD+(1-QC)*QSD*(1-.5*(1-QC)*QSD))*(1-QK)
00460     S(2,K)=1-S(1,K)-S(3,K)-S(4,K)
00470 IF(IX.EQ.1)GO TO 10
00480     OTM(1,1)=S(1,3)/S(1,1)  ;  CTM(1,1)=S(1,4)/S(1,2)
00490     OTM(1,3)=(S(3,3)-S(3,1))/(S(1,1)+S(2,1))
00500     OTM(1,4)=(S(4,3)-S(4,1))/(S(1,1)+S(2,1))
00510     OTM(1,2)=1-OTM(1,1)-OTM(1,3)-OTM(1,4)
00520     OTM(2,3)=OTM(1,3)  ;  OTM(2,4)=OTM(1,4)
00530     OTM(2,2)=1-OTM(2,3)-OTM(2,4)
00540     OTM(3,3)=1  ;  OTM(4,4)=1
00550     CTM(1,3)=(S(3,4)-S(3,2))/(S(1,2)+S(2,2))
00560     CTM(1,4)=(S(4,4)-S(4,2))/(S(1,2)+S(2,2))
00570     CTM(1,2)=1-CTM(1,1)-CTM(1,3)-CTM(1,4)
00580     CTM(2,3)=CTM(1,3)  ;  CTM(2,4)=CTM(1,4)
00590     CTM(2,2)=1-CTM(2,3)-CTM(2,4)
00600     CTM(3,3)=1 ; CTM(4,4)=1
```

* * * *

Table A-14. Power Subsystem Reliability Program (Cont)

* * * *

FILE TSS-REL LISTING PAGE 03

```
00610 DO 20 KT=1,4 ; DO 20 K12=1,2
00620 UTMA(KT,K12)=SMA(KT,K12)
00630 20 SMA(KT,K12)=0
00640 DO 21 KT=1,4  ;  DO 21 KKT=1,4
00650 SMA(KT,1)=SMA(KT,1)+UTMA(KKT,1)*CTM(KKT,KT)
00660 21 SMA(KT,2)=SMA(KT,2)+UTMA(KKT,2)*CTM(KKT,KT)
00670 SMA(1,2)=SMA(1,2)+SMA(1,1)*P12
00680 SMA(3,2)=SMA(3,2)+SMA(3,1)*.5*P12
00690 SMA(4,2)=SMA(4,2)+SMA(2,1)*P12
00700 SMA(1,1)=SMA(1,1)*(1-P12)
00710 SMA(2,1)=SMA(2,1)*(1-P12)
00720 SMA(3,1)=SMA(3,1)*(1-P12)
00730 SMA(4,1)=SMA(4,1)*(1-P12)
00740 DO 24 N=1,2  ;  SUM=0
00750 DO 26 M=1,4 ;  26 SUM=SUM+SMA(M,N)
00760 24 PM(N)=1/SUM
00770 DO 25 N=1,2 ; DO 25 M=1,4
00780 25 UTMA(M,N)=PM(N)*SMA(M,N)
00790 RSTSW=EXP(-T*YSTSW/1000000)
00800 PNO=YOSTSW*(1-RSTSW) ; PWO=1-RSTSW-PNO
00810 RDTPWO=(1-PWO)/(1-PWO1)  ;  PWO1=PWO
00820 RDCT=DEXP(-T*YCT/10/1000000)
00830 PSDCT=(1-YOCT)*(1-RDCT)
00840 PFO2=UTMA(3,1)
00850 RDTFO=(1-PFO2)/(1-PFO1)  ;  PFO1=PFO2
00860 PSWOVER=UTMA(1,1)+UTMA(2,1)
00870 SSTT(1,1)=RCT*RDTPWO*RDTFO
00880 SSTT(1,2)=PSCT*RDTFO*PNO
00890 SSTT(1,3)=(1-RDTPWO+(1-RDTFO+1-RCT)*RSTSW)*RDCT*PSWOVER
00900 SSTT(1,4)=SSTT(1,3)/RDCT*PSDCT
```

* * * *

Table A-14. Power Subsystem Reliability Program (Cont)

* * * *


```
00910 SSTT(1,5)=1-SSTT(1,1)-SSTT(1,2)-SSTT(1,3)-SSTT(1,4)
00920 SSTT(2,2)=RDTF0
00950 SSTT(2,5)=1-SSTT(2,2)-SSTT(2,3)-SSTT(2,4)
00960 P12=(SSSM(1)*(SSTT(1,3)+SSTT(1,4))+SSSM(2)*(SSTT(2,3)+
00970 &SSTT(2,4)))/(SSSM(1)+SSSM(2))
00980 PF202=UTMA(3,2)
00990 RDTF02=(1-PF202)/(1-PF201)  ;  PF201=PF202
01000 SSTT(3,3)=RCT*RDTF02
01010 SSTT(3,4)=PSCT*RDTF02
01020 SSTT(3,5)=1-SSTT(3,3)-SSTT(3,4)
01030 SSTT(4,4)=RDTF02
01040 SSTT(4,5)=1-SSTT(4,4)
01050 DO 31 KSS=1,5  ;  NSSSM(KSS)=SSSM(KSS)
01060 31 SSSM(KSS)=0
01070 DO 32 KSS=1,5 ; DO 32 KKSS=1,5
01080 32 SSSM(KSS)=SSSM(KSS)+NSSSM(KKSS)*SSTT(KKSS,KSS)
01090 IF(KK.LT.NIT/10)GO TO 10  ;  KK=0
01100 I=IX/100
01110 ** C T FUNCTION
01120 PCTPOW=1-SSSM(5)
01130 PCTG=SSSM(1)+SSSM(3)+SSSM(2)*RSTSW*PSWOVER*RDCT
01140 ** DIODE FUNCTION
01150 RDIOD=DEXP(-T*YDIOD/1000000)
01160 PODIOD=YODIOD*(1-RDIOD)
01170 RPD=(1-PODIOD**2)**4
01180 ** RTG FUNCT
01190 RRTG=EXP(-T*YRTG/1000000)
01200 PGRTG=RRTG**4
01210 *** POWER DELIVERY
01220 P100POW=PGRTG*RPD*PCTPOW*RSHUNT(I)*RMINV(I)
```

* * * *

Table A-14. Power Subsystem Reliability Program (Cont)

* * * *

FILE TSS-REL LISTING 01/04/72 PAGE 05

```
01230 *** FAILURE HANDLING OK
01240 PFTOL=PGRTG*RPD*PCTG*RSHUNT(I)*RMINV(I)*RPINV(I)
01250 TY=T/24/365.25
01260 PRINT 100,TY,P100POW,PFTOL
01270 IF(IX.EQ.NIT)ASK="YES"
01280 IF(ASK.NE."YES")GO TO 10
01285 PRINT:" " ; PRINT:" "
01290 PRINT:"      PGRTG   CT PATH   CT GOOD  POW DIODES"
01300 PRINT 101,PGRTG,PCTPOW,PCTG,RPD
01310 PRINT:"  C.T. STATE MATRIX"
01320 PRINT 101,(SSSM(M),M=1,5)
01330 PRINT:"  C.T. TRANSITION MATRIX"
01340 PRINT 101,((SSTT(N,M),M=1,5),N=1,5)
01350 10 CONTINUE
01360 100 FORMAT(1H0,F5.2," YEARS",/,1H ,"MAIN BUS 100% POWER REL=",
01370 &F9.6,/,1H ,"FAILURE TOLERANT REL   =",F9.6)
01380 101 FORMAT(2H  ,5F10.7)
01390 STOP
01400 END
END OF FILE TSS-REL
```

APPENDIX B
TRANSFORMER ANALYSIS

Table B-1. Transformer Analysis Program

```
00010 *  TRANSFORMER ANALYSIS   T.J.E. 2/2/70
00020 *  STATEMENTS 8-30
00030 *
00040 * FORMATS 99-107,111-114
00050 DIMENSION XM(4,4),XK(4,4),FLUX(4,4),WF(4),APOW(5),AWT(5),AVE(4),
00060 &HZ(4),NFSKIP(4),CRO(4),V(6),A(6),N(6),KIND(6)
00070 ASCII ASC(10),DATE(2)
00080 PI=3.14159
00090 CALL DATE#TIM(DATE,HOUR) ; PRINT 99,DATE,HOUR
00100 PRINT:"  TRANSFORMER ANALYSIS-WEIGHT,POWER,EFFICIENCY MATRIX"
00110 PRINT:"   RUN I.D." ; READ:ASC(10)
00120 PRINT:" "; PRINT:"  DO YOU WANT DETAILED PRINTOUT?" ; READ:ASC(1)
00130 PRINT:"PUT IN UP TO 6 WINDINGS,IN ORDER FROM CORE OUTWARD"
00140 PRINT:" NUMBER OF WINDINGS,WHICH WINDING IS PRIMARY?" ; READ:NW,NF
00150 PRINT:" VOLTS,AMPS,KIND(2=CT) OF ALL WINDINGS" ; PRINT:" "
00160 READ:(V(K),A(K),KIND(K),K=1,NW)
00170 PRINT:"PUT IN 4 FLUXES FOR EACH CORE TYPE,0 MUST BE USED IF
00180 & REAL FLUX NOT DESIRED"
00190 PRINT:"      (1)ORTHANOL,(2)48 ALLOY,(3)SUPERMALLOY,(4) C CORE"
00200 PRINT:" FLUXES" ; READ:((FLUX(I,K),K=1,4),I=1,4)
00210 PRINT:" FREQUENCIES NOT DESIRED(1,2,3,&/OR 4)"; READ:(NFSKIP(I),I=1
,4)
00220 PRINT:"  MINIMUM CORE DIMENSION" ; READ:D0
00230 PRINT:"  % WINDOW AREA USABLE FOR EACH MATERIAL"; READ:(WF(I),I=1,4
)
00240 PRINT:" COPPER-STACKING FACTOR,RESISTIVITY(MICRO-OHM IN2/IN),
```

Table B-1. Transformer Analysis Program (Cont'd)

```
00250 &WEIGHT(LBS/IN3)," ; PRINT:" AND MAX CURRENT DENSITY(AMPS/IN2)"
00260 READ:SF,SIGMA,CURO,ASIMAX ; SIGMA=SIGMA*1.0E-6
00270 PRINT:" SWITCH DATA-VSAT,RISE,&FALL TIME(MICRO SECONDS)"
00280 READ:TR,TF  ;  TR=TR*1.0E-6  ;  TF=TF*1.0E-6
00290 PRINT:" WATTS/POUND FACTOR(0 FOR MATRIX),MAX VOLTS/TURN"
00300 READ:PF,VPTMAX
00310 *  SLOPES AND INTERCEPTS FOR CORE LOSSES
00320 XM(1,1)=1.32;XM(1,2)=1.23;XM(1,3)=1.11;XM(1,4)=1.03
00330 XK(1,1)=-.73;XK(1,2)=.03; XK(1,3)=.55 ; XK(1,4)=.875
00340 XM(2,1)=1.62;XM(2,2)=1.61;XM(2,3)=1.58;XM(2,4)=1.45
00350 XK(2,1)=-1.17;XK(2,2)=-.41;XK(2,3)=0.08;XK(2,4)=.53
00360 XM(3,1)=2.00;XM(3,2)=1.96;XM(3,3)=1.91;XM(3,4)=1.78
00370 *   CORE DENSITIES(#/IN3)
00380 XK(3,1)=-1.76;XK(3,2)=-1.15;XK(3,3)=-.66;XK(3,4)=-.35
00390 XM(4,1)=1.80;XM(4,2)=1.77;XM(4,3)=1.94;XM(4,4)=2.00
00400 XK(4,1)=-.48;XK(4,2)=-.22;XK(4,3)=.20 ; XK(4,4)=.55
00410 CRO(1)=8.2*.03613*.89
00420 CRO(2)=8.2*.03613*.89
00430 CRO(3)=8.7*.03613*.89
00440 CRO(4)=.276*.83
00450 HZ(1)=1000 ; HZ(2)=3000 ; HZ(3)=6000 ; HZ(4)=10000
00460 POUT=0 ; DO 14 J=1,NW ; IF(J.EQ.NP) GO TO 14
00470 POUT=POUT+A(J)*V(J) ; 14 CONTINUE
00480 NPRINT=11
00490 DO 15 I=1,4
00500 IF(I.EQ.4)HZ(2)=2000  ;  IF(I.EQ.4)HZ(3)=5000
00510 IF(I.EQ.1)PRINT 111
00520 IF(I.EQ.2)PRINT 112 ; IF(I.EQ.3)PRINT 113 ; IF(I.EQ.4)PRINT 114
```

Table B-1. Transformer Analysis Program (Cont'd)

```
00530 PRINT 105, WF(I)
00540 CORRO=CRO(I)
00550 DO 17 M=1,4
00560 B=FLUX(I,M)
00570 IF(B.EQ.0) GO TO 17
00580 DO 16 K=1,4
00590 IF(K.EQ.NFSKIP(1)) GO TO 16 ; IF(K.EQ.NFSKIP(2)) GO TO 16
00600 IF(K.EQ.NFSKIP(3)) GO TO 16 ; IF(K.EQ.NFSKIP(4)) GO TO 16
00610 XLOGCL=XM(I,K)*(.43429*ALOG(B)-3.0)+XK(I,K)
00620 WPLB=EXP(2.30258*XLOGCL)
00630 FREQ=HZ(K)
00640 PRINT 104, B, FREQ, WPLB
00650 KIKWT=0 ; KIKPOW=0 ; IAVE=0 ; KIKPF=0
00660 TWT0=0.  ;  TPOW0=0.  ;  TWO=2.00
00670 D=D0  ;  D1=0.  ;  DX=0
00680 9 CONTINUE
00690 D=SQRT(1.001*D*D)
00700 IF(DX.EQ.0) D=SQRT(D*D*(1.+.049/1.001))
00710 R1=2.0*D ; RO=3.0*D
00720 ACORE=D*2.*D*6.425  ;  IF(I.EQ.4) ACORE=D*1.5*D*6.425
00730 CORVOL=10.*PI*D*D*D ; IF(I.EQ.4) CORVOL=24.*D*D*D
00740 CORWT=CORVOL*CORRO  ;  CORPOW=CORWT*WPLB
00750 VPT=(ACORE*B/1000.*FREQ/1000.)/25. ; N(NP)=V(NP)/VPT
00760 IF(VPT.GT.VPTMAX)KIKPOW=1
00770 A(NP)=0  ;  CA=0
00780 IF(N(NP).LT.2) GO TO 12
00790 DO 8 J=1,NW
00800 IF(J.EQ.NP) GO TO 8
```

Table B-1. Transformer Analysis Program (Cont'd)

```
00810 XN=V(J)*N(NP)/V(NP)  ;  N(J)=XN
00820 IF((XN-IFIX(XN)).GT.0.5)N(J)=N(J)+1
00830 A(NP)=A(NP)+N(J)*A(J)/N(NP)
00840 IF(N(J).LT.2)GO TO 12
00850 8 CONTINUE
00860 AW=PI*R1*R1*SF*WF(I)/100.
00870 IF(I.EQ.4)AW=1.5*D*4.5*D*SF*WF(I)/100.
00880 DO 10 J=1,NW
00890 10 CA=CA+KIND(J)*N(J)*A(J)
00900 ASI=CA/AW
00910 1919 FORMAT(1H ,I8,F6.2,I8,E13.5,2F8.3,E13.5)
00920 ASI=CA/AW ; IF(ASI.GT.ASIMAX)GO TO 9 ; CUPOW=0
00930 IF(DX.NE.0)GO TO 22
00940 D=SQRT(D*D*.957)  ;  DX=D  ;  GO TO 9
00950 22 IF(D1.EQ.0)D1=.999999*D ; XL1=D
00960 XL1=D ; XLL1=1.5*D ; XLI1=2.*D ; XLO1=2.*D
00970 DO 11 J=1,NW
00980 CADEL=KIND(J)*N(J)*A(J)/ASI
00990 ADEL=CADEL/SF
01000 IF(I.EQ.4)GO TO 27
01010 R2=SQRT(R1*R1-ADEL/PI) ; RO2=SQRT(RO*RO+ADEL/PI)
01020 XL2=XL1+R1-R2+RO2-RO
01030 XLO2=XLO1+2.*(RO2-RO) ; XLI2=XLI1+2.*(R1-R2)
01040 XMLT=(XLI1+XLI2+XLO1+XLO2)/2.+XL1+XL2
01050 XL1=XL2 ; XLI1=XLI2 ; XLO1=XLO2 ; R1=R2 ; RO=RO2
01060 GO TO 28
01070 27 XL2=XL1+2.*ADEL/(4.5*D) ; XLL2=XLL1+2.*ADEL/(4.5*D)
01080 XMLT=XL1+XL2+XLL1+XLL2
```

Table B-1. Transformer Analysis Program (Cont'd)

```
01090 XL1=XL2 ; XLL1=XLL2
01100 28 CONTINUE
01110 CUPOW=CUPOW+SIGMA*XMLT*(A(J)*N(J))**2./(CADEL/KIND(J))
01120 11 CONTINUE
01130 SLOPE=(XLI2-XLO2)/XL2
01140 CUVOL=PI*((XLI2+R2*SLOPE)*(RO2*RO2-R2*R2)-2.*SLOPE/3.*(RO**3.-
01150 &R2**3.))-10.*PI*D*D*D
01160 IF(I.EQ.4)CUVOL=XL2*XLL2*4.5*D-6.75*D*D*D
01170 CUWT=CUVOL*SF*CURO
01180 SLPOW=2./3.*2.*V(NP)*A(NP)*(TF+TR)*FREQ+VCESAT*A(NP)
01190 TWT=CORWT+CUWT ;  TPOW=CORPOW+CUPOW+SLPOW
01200 IF(TWT.GT.90)GO TO 12
01210 IF(TWT0.EQ.0)TWT0=TWT ; IF(TWT.GT.1.001*TWT0)KIKWT=1
01220 IF(TPOW0.EQ.0)TPOW0=TPOW ; IF(TPOW.GT.1.001*TPOW0)KIKPOW=1
01230 IF(D.GT.100*D1)GO TO 12
01240 IF(PF.EQ.0)GO TO 25
01250 IAVE=IAVE+1 ; IF(IAVE.EQ.6)IAVE=1
01260 APOW(IAVE)=TPOW ; AWT(IAVE)=TWT
01270 IF(KIKPF.EQ.0)GO TO 23
01280 I1=IAVE+1
01290 XAVE=0
01300 DO 24 MAVE=1,4
01310 I1=I1-1 ; IF(I1.EQ.0)I1=5
01320 I2=I1-1 ; IF(I1.EQ.1)I2=5
01330 AVE(MAVE)=(APOW(I1)-APOW(I2))/(AWT(I2)-AWT(I1))
01340 24 XAVE=XAVE+AVE(MAVE)
01350 IF(XAVE/4..LT.PF)D=D*1.002001/1.004006
01360 IF(XAVE/4..LT.PF)D1=D
```

Table B-1. Transformer Analysis Program (Cont'd)

```
01370 23 IF(IAVE.EQ.4)KIKPF=1
01380 NPRINT=1
01390 IF(KIKPOW.EQ.1)D1=D
01400 IF(D1.EQ.D)GO TO 12
01410 GO TO 9
01420 25 CONTINUE
01430 IF(KIKPOW.EQ.0)GO TO 9
01440 IF(D.LT.1.26*D1)D=1.26*D1
01450 12 IF(D1.EQ.0)GO TO 13 ; XD=ALOG(D/D1)/10.
01460 IF(ASC(1).EQ."YES")PRINT 107 ,D,D1,XD
01470 IF(PF.NE.0)PRINT 106,XAVE/4.
01480 DO 13 JF=1,NPRINT
01490 IF(JF.GT.1)GO TO 26
01500 PRINT 102 ; IF(ASC(1).EQ."YES")PRINT 103
01510 26 D=EXP(ALOG(D1)+(JF-1)*XD)
01520 R1=2.*D  ;  RO=3.*D
01530 ACORE=D*2.*D*6.425 ; IF(I.EQ.4)ACORE=D*1.5*D*6.425
01540 CORVOL=10.*PI*D*D*D ; IF(I.EQ.4)CORVOL=24.*D*D*D
01550 CORWT=CORVOL*CORRO  ;  CORPOW=CORWT*WPLB
01560 VPT=(ACORE*B/1000.*FREQ/1000.)/25. ; N(NP)=V(NP)/VPT
01570 A(NP)=0  ;  CA=0
01580 DO 18 J=1,NW
01590 IF(J.EQ.NP)GO TO 18
01600 XN=V(J)*N(NP)/V(NP)  ;  N(J)=XN
01610 IF((XN-IFIX(XN)).GT.0.5)N(J)=N(J)+1
01620 A(NP)=A(NP)+N(J)*A(J)/N(NP)
01630 IF(N(J).LT.1)PRINT:"N=",N(J)," JF=",JF
01640 IF(N(J).LT.1)N(J)=1
```

Table B-1. Transformer Analysis Program (Cont'd)

```
01650 18 CONTINUE
01660 AW=PI*R1*R1*SF*WF(I)/100.
01670 IF(I.EQ.4)AW=1.5*D*4.5*D*SF*WF(I)/100.
01680 DO 20 J=1,NW
01690 20 CA=CA+KIND(J)*N(J)*A(J)
01700 ASI=CA/AW ; CUPOW=0
01710 XL1=D ; XLL1=1.5*D ; XLI1=2.*D ; XLO1=2.*D
01720 DO 21 J=1,NW
01730 CADEL=KIND(J)*N(J)*A(J)/ASI
01740 ADEL=CADEL/SF ; IF(I.EQ.4)GO TO 29
01750 R2=SQRT(R1*R1-ADEL/PI) ; RO2=SQRT(RO*RO+ADEL/PI)
01760 XL2=XL1+R1-R2+RO2-RO
01770 XLI2=XLI1+2.*(R1-R2) ; XLO2=XLO1+2.*(RO2-RO)
01780 XMLT=(XLI1+XLI2+XLO1+XLO2)/2.+XL1+XL2
01790 XL1=XL2 ; XLI1=XLI2 ; XLO1=XLO2 ; R1=R2 ; RO=RO2
01800 GO TO 30
01810 29 XL2=XL1+2.*ADEL/(4.5*D) ; XLL2=XLL1+2.*ADEL/(4.5*D)
01820 XMLT=XL1+XL2+XLL1+XLL2
01830 XL1=XL2 ; XLL1=XLL2
01840 30 CONTINUE
01850 CUPOW=CUPOW+SIGMA*XMLT*(A(J)*N(J))**2./(CADEL/KIND(J))
01860 21 CONTINUE
01870 SLOPE=(XLI2-XLO2)/XL2
01880 CUVOL=PI*((XLI2+R2*SLOPE)*(RO2*RO2-R2*R2)-2.*SLOPE/3.*(RO2**3.-
01890 &R2**3.))-10.*PI*D*D*D
01900 IF(I.EQ.4)CUVOL=XL2*XLL2*4.5*D-6.75*D*D*D
01910 CUWT=CUVOL*SF*CURO
```

Table B-1. Transformer Analysis Program (Cont'd)

```
01920 SLPOW=2./3.*2.*V(NP)*A(NP)*(TK+TF)*FREQ*VCESAT*A(NP)
01930 TWT=CORWT+CUWT  ;  TPOW=CORPOW+CUPOW+SLPOW
01940 EFF=POUT/(POUT+TPOW)
01950 PRINT 100,TWT,TPOW,EFF ; IF(ASC(1).EQ."YES")PRINT 101,CORWT,CUWT,
01960 &CORPOW,CUPOW,ASI,D,VPT
01970 13 CONTINUE
01980 16 CONTINUE
01990 17 CONTINUE
02000 15 CONTINUE
02010 CALL DATE#TIM(DATE,HOUR) ; PRINT 99,DATE,HOUR
02020 99 FORMAT(1H0,2A4,F7.3)
02030 100 FORMAT(1H ,3F6.3)
02040 101 FORMAT(1H&,4F6.3,F7.0,2F6.3)
02050 102 FORMAT(1H0,"     WT    POW    EFF")
02060 103 FORMAT(1H&," CORWT  CUWT  CPOW CUPOW     ASI      D")
02070 104 FORMAT(1H-,"GAUSS=",F8.0,"     FREQUENCY=",F8.0,"     CORE LOSS=
",
02080 &F7.3," WATTS/LB")
02090 105 FORMAT(1H ," WINDOW AREA USED",F5.0," %")
02100 106 FORMAT(1H ," D WATTS/D POUNDS AVE=",F7.3," WATTS/POUND")
02110 107 FORMAT(1H ," FINAL D=",F7.3," IN.      D1=",F7.3," IN.
02120 &      KD=",F7.4)
02130 111 FORMAT(1H-,/,1H-,20(1H*)," 2 MIL ORTHONOL ",20(1H*))
02140 112 FORMAT(1H-,/,1H-,20(1H*)," 2 MIL 48 ALLOY ",20(1H*))
02150 113 FORMAT(1H-,/,1H-,20(1H*)," 2 MIL SUPERMALLOY ",17(1H*))
02160 114 FORMAT(1H-,/,1H-,20(1H*)," 1 MIL SELECTRONIC C CORE ",10(1H*))
02170 STOP
02180 END
```

Table B-2. Transformer Analysis Printout

```
   TRANSFORMER ANALYSIS-WEIGHT,POWER,EFFICIENCY MATRIX
    RUN I.D.=HI WT ORTH & SUPMLY TOROIDS  & SUPCIL C CORE


   DO YOU WANT DETAILED PRINTOUT?=YES

PUT IN UP TO 6 WINDINGS,IN ORDER FROM CORE OUTWARD
 NUMBER OF WINDINGS,WHICH WINDING IS PRIMARY?= 3, 2

 VOLTS,AMPS,KIND(2=CT) OF ALL WINDINGS
 = 6.4, 3.15, 2,     29.56, 0, 2,     32.64, 0.1, 1

PUT IN 4 FLUXES FOR EACH CORE TYPE,0 MUST BE USED IF REAL FLUX NOT
     (1)ORTHANOL,(2)48 ALLOY,(3)SUPERMALLOY,(4) C CORE
 FLUXES=2000,1000,0,0,  0,0,0,0,  2000,1000,500,0,   1500,1000,500,0,

 FREQUENCIES NOT DESIRED(1,2,3,&/OR 4)=1,2,0,4

  MINIMUM CORE DIMENSION=.12

  % WINDOW AREA USABLE FOR EACH MATERIAL= 70, 70, 70, 90

 COPPER-STACKING FACTOR,RESISTIVITY(MICRO-OHM IN2/IN),WEIGHT(LBS/IN3),
 AND MAX CURRENT DENSITY(AMPS/IN2)= 0.6, 0.68, 0.32, 3000

 SWITCH DATA-VSAT,RISE,&FALL TIME(MICRO SECONDS)= 0.25, 1, 1

 WATTS/POUND FACTOR(0 FOR MATRIX),MAX VOLTS/TURN= 0, 0.2

********** 2 MIL ORTHONOL **********
 WINDOW AREA USED  70. %


GAUSS=   2000.    FREQUENCY=   6000.    CORE LOSS=  7.658 WATTS/LB
 FINAL D=  0.220 IN.     D1=  0.174 IN.     XD= 0.0231

    WT    POW    EFF  CORWT  CUWT  CPOW CUPOW    ASI     D
 0.122 1.334 0.946 0.044 0.078 0.335 0.765  2998.   0.174   0.187
 0.131 1.256 0.949 0.047 0.084 0.360 0.665  2700.   0.178   0.196
 0.140 1.227 0.950 0.050 0.090 0.385 0.607  2493.   0.182   0.205
 0.150 1.203 0.951 0.054 0.096 0.413 0.554  2300.   0.187   0.215
 0.161 1.149 0.953 0.058 0.103 0.443 0.475  2056.   0.191   0.225
 0.173 1.138 0.954 0.062 0.111 0.474 0.430  1890.   0.196   0.236
 0.185 1.133 0.954 0.066 0.119 0.509 0.388  1736.   0.200   0.247
 0.198 1.133 0.954 0.071 0.127 0.545 0.351  1593.   0.205   0.259
 0.213 1.137 0.954 0.076 0.136 0.584 0.315  1459.   0.210   0.271
 0.228 1.148 0.953 0.082 0.146 0.626 0.283  1335.   0.215   0.284
 0.244 1.134 0.954 0.088 0.157 0.671 0.233  1169.   0.220   0.297
```

Table B-2. Transformer Analysis Printout (Cont'd)

```
********************* 2 MIL SUPERMALLOY *****************
 WINDOW AREA USED  70. %

GAUSS=    2000.     FREQUENCY=    6000.     CORE LOSS=  0.822 WATTS/LB
 FINAL D=   0.220 IN.      D1=   0.174 IN.      XD= 0.0231

    WT    POW    EFF CORWT  CUWT  CPOW CUPOW    ASI      D
 0.125 1.037 0.958 0.046 0.078 0.038 0.765  2998.   0.174   0.187
 0.134 0.938 0.962 0.050 0.084 0.041 0.665  2700.   0.178   0.196
 0.143 0.886 0.964 0.053 0.090 0.044 0.607  2493.   0.182   0.205
 0.154 0.838 0.965 0.057 0.096 0.047 0.554  2300.   0.187   0.215
 0.165 0.757 0.969 0.061 0.103 0.050 0.475  2056.   0.191   0.225
 0.176 0.718 0.970 0.066 0.111 0.054 0.430  1890.   0.196   0.236
 0.189 0.682 0.972 0.070 0.119 0.058 0.388  1736.   0.200   0.247
 0.203 0.650 0.973 0.076 0.127 0.062 0.351  1593.   0.205   0.259
 0.217 0.619 0.974 0.081 0.136 0.067 0.315  1459.   0.210   0.271
 0.233 0.593 0.975 0.087 0.146 0.071 0.283  1335.   0.215   0.284
 0.250 0.539 0.977 0.093 0.157 0.076 0.233  1169.   0.220   0.297

GAUSS=    1000.     FREQUENCY=    6000.     CORE LOSS=  0.219 WATTS/LB
 FINAL D=   0.261 IN.      D1=   0.207 IN.      XD= 0.0231

    WT    POW    EFF CORWT  CUWT  CPOW CUPOW    ASI      D
 0.210 1.535 0.939 0.078 0.131 0.017 1.285  2998.   0.207   0.132
 0.225 1.404 0.943 0.084 0.141 0.018 1.152  2743.   0.212   0.139
 0.241 1.283 0.948 0.090 0.151 0.020 1.029  2504.   0.217   0.145
 0.258 1.172 0.952 0.096 0.162 0.021 0.916  2282.   0.222   0.152
 0.276 1.069 0.956 0.103 0.173 0.023 0.812  2076.   0.227   0.159
 0.296 0.974 0.960 0.110 0.186 0.024 0.718  1884.   0.232   0.167
 0.318 0.925 0.962 0.118 0.199 0.026 0.662  1749.   0.238   0.175
 0.340 0.843 0.965 0.127 0.214 0.028 0.580  1581.   0.243   0.183
 0.365 0.767 0.968 0.136 0.229 0.030 0.505  1425.   0.249   0.191
 0.391 0.729 0.970 0.146 0.245 0.032 0.462  1317.   0.255   0.200
 0.419 0.666 0.972 0.156 0.263 0.034 0.399  1181.   0.261   0.210

GAUSS=     500.     FREQUENCY=    6000.     CORE LOSS=  0.058 WATTS/LB
 FINAL D=   0.360 IN.      D1=   0.246 IN.      XD= 0.0379

    WT    POW    EFF CORWT  CUWT  CPOW CUPOW    ASI      D
 0.353 2.407 0.907 0.132 0.222 0.008 2.165  2997.   0.246   0.094
 0.396 2.031 0.920 0.148 0.248 0.009 1.789  2574.   0.256   0.101
 0.444 1.752 0.930 0.165 0.278 0.010 1.507  2232.   0.266   0.109
 0.497 1.463 0.941 0.185 0.312 0.011 1.219  1896.   0.276   0.118
 0.557 1.251 0.949 0.208 0.350 0.012 1.006  1627.   0.287   0.127
 0.624 1.102 0.955 0.233 0.392 0.014 0.852  1415.   0.298   0.137
 0.699 0.938 0.961 0.261 0.439 0.015 0.690  1203.   0.309   0.148
 0.784 0.825 0.966 0.292 0.492 0.017 0.574  1036.   0.321   0.159
 0.878 0.726 0.970 0.327 0.551 0.019 0.473   889.   0.334   0.172
 0.984 0.639 0.973 0.367 0.617 0.021 0.386   758.   0.347   0.185
 1.103 0.586 0.976 0.411 0.692 0.024 0.327   660.   0.360   0.200
```

Table B-2. Transformer Analysis Printout (Cont'd)

```
********************* 1 MIL SELECTRONIC C CORE **********
 WINDOW AREA USED  90. %

GAUSS=    1500.     FREQUENCY=    5000.     CORE LOSS=  3.480 WATTS/LB
 FINAL D=  0.291 IN.      D1=  0.231 IN.      XD= 0.0231

    WT    POW    EFF CORWT  CUWT  CPOW CUPOW    ASI     D
 0.217 1.920 0.924 0.068 0.149 0.235 1.490  2986.  0.231  0.154
 0.232 1.828 0.928 0.072 0.160 0.252 1.379  2776.  0.236  0.161
 0.249 1.684 0.933 0.078 0.171 0.270 1.217  2518.  0.242  0.169
 0.267 1.554 0.938 0.083 0.184 0.290 1.070  2281.  0.247  0.177
 0.286 1.440 0.942 0.089 0.197 0.310 0.936  2059.  0.253  0.185
 0.307 1.386 0.944 0.096 0.211 0.333 0.858  1905.  0.259  0.194
 0.329 1.292 0.948 0.103 0.226 0.357 0.742  1711.  0.265  0.203
 0.352 1.254 0.949 0.110 0.242 0.382 0.676  1578.  0.271  0.213
 0.378 1.224 0.950 0.118 0.260 0.410 0.616  1456.  0.278  0.223
 0.405 1.158 0.953 0.126 0.278 0.439 0.525  1297.  0.284  0.234
 0.434 1.141 0.954 0.135 0.298 0.471 0.475  1192.  0.291  0.245

GAUSS=    1000.     FREQUENCY=    5000.     CORE LOSS=  1.585 WATTS/LB
 FINAL D=  0.323 IN.      D1=  0.256 IN.      XD= 0.0231

    WT    POW    EFF CORWT  CUWT  CPOW CUPOW    ASI     D
 0.297 2.336 0.909 0.093 0.204 0.147 1.995  2951.  0.256  0.127
 0.318 2.146 0.916 0.099 0.219 0.157 1.793  2703.  0.262  0.133
 0.341 1.972 0.922 0.106 0.235 0.169 1.608  2473.  0.269  0.139
 0.366 1.814 0.928 0.114 0.252 0.181 1.438  2259.  0.275  0.146
 0.392 1.669 0.933 0.122 0.270 0.194 1.279  2058.  0.281  0.152
 0.420 1.538 0.938 0.131 0.289 0.208 1.135  1872.  0.288  0.160
 0.450 1.419 0.943 0.140 0.310 0.223 1.001  1699.  0.295  0.167
 0.483 1.313 0.947 0.151 0.332 0.239 0.881  1538.  0.301  0.175
 0.517 1.262 0.949 0.161 0.356 0.256 0.810  1426.  0.308  0.183
 0.554 1.174 0.952 0.173 0.382 0.274 0.705  1284.  0.316  0.192
 0.594 1.136 0.954 0.185 0.409 0.294 0.645  1187.  0.323  0.201

GAUSS=     500.     FREQUENCY=    5000.     CORE LOSS=  0.413 WATTS/LB
 FINAL D=  0.456 IN.      D1=  0.304 IN.      XD= 0.0403

    WT    POW    EFF CORWT  CUWT  CPOW CUPOW    ASI     D
 0.497 3.644 0.865 0.155 0.342 0.064 3.386  2972.  0.304  0.089
 0.561 3.074 0.884 0.175 0.386 0.072 2.807  2547.  0.317  0.097
 0.633 2.577 0.901 0.198 0.436 0.082 2.300  2171.  0.330  0.105
 0.715 2.151 0.916 0.223 0.492 0.092 1.864  1839.  0.344  0.114
 0.807 1.842 0.927 0.252 0.555 0.104 1.542  1575.  0.358  0.123
 0.911 1.575 0.937 0.284 0.627 0.117 1.262  1341.  0.372  0.134
 1.028 1.347 0.946 0.321 0.707 0.132 1.019  1134.  0.388  0.145
 1.160 1.195 0.951 0.362 0.798 0.149 0.849   975.  0.404  0.157
 1.309 1.029 0.958 0.408 0.901 0.169 0.667   813.  0.420  0.170
 1.478 0.958 0.961 0.461 1.017 0.190 0.570   708.  0.438  0.185
 1.668 0.869 0.964 0.520 1.148 0.215 0.458   597.  0.456  0.200
```